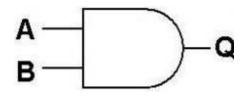
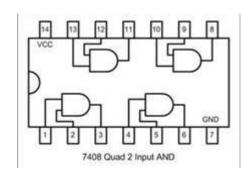
# UCI Critter Study Group 2021 Applied Robotics & Embedded Programming

# **Working With Digital Logic Gates**

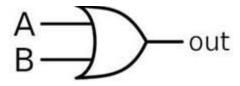
### 7408 AND Gate



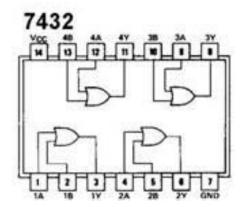
2 Input AND gate		
Α	В	A.B
0	0	0
0	1	0
1	0	0
1	1	1





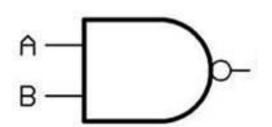


A	В	out
0	0	0
0	1	1
1	0	1
1	1	1



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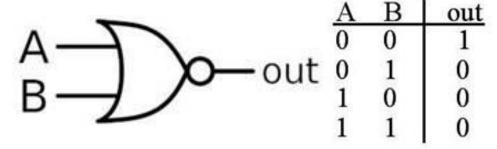
## NAND Gate 7400 or 4011



A	В	out
0	0	1
0	1	1
1	0	1
1	1	0

**NAND Gate Truth Table** 

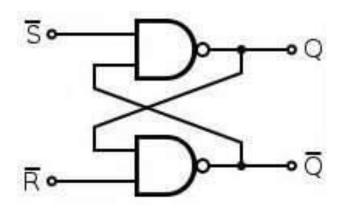
### NOR Gate 7402 or 4001

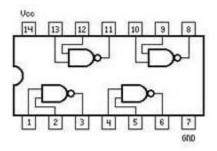


**NOR Gate Truth Table** 

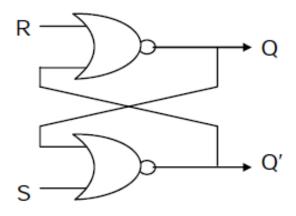
# Introduction to the S-R Latch or S-R flip-flop

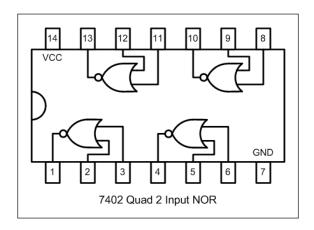
S-R Latch Using7400 NAND Gates. This is called an Active Low latch because a low pulse on Set or Reset activates it.





S-R Latch Using 7402 NOR Gates. This is called an Active High latch because a high pulse on Set or Reset activates it.





### Figure 1. RS Latch in Set or Latched Mode

Top trace is Q. The bottom trace shows me triggering the Set input. Only the first pulse on Set will actually set the latch. The other pulses do not.

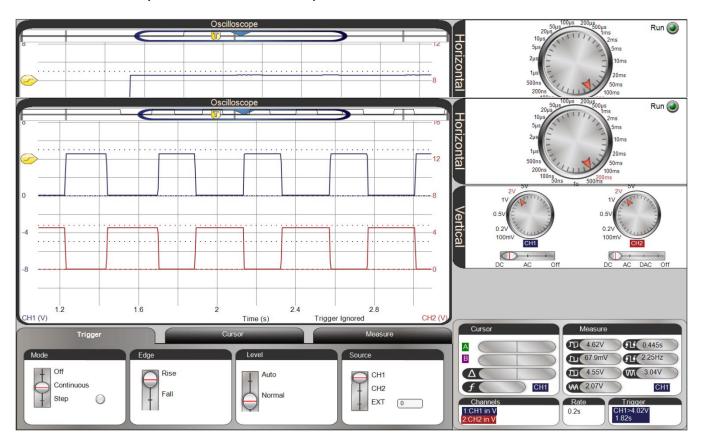


Figure 2 Comparison of Q and  $\bar{Q}$ . Note how they are inversely related.

The top trace is Q and the bottom trace is  $\bar{Q}$ .

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Now let's build one! You may create either an Active Low or Active High RS latch. Be sure to check your pin outs for the chip you are using. The resistors on the inputs are called "Pull-Ups" when connected to B+ because they hold those inputs High. The resistors that hold inputs Low are called "Pull-Downs". These resistors are typically 2,000 – 10,000 ohms. For this exercise, go ahead and use the values in the schematic (10K Brown-Black-Orange).

Also, use a Green LED for the Set condition and a Red LED for Reset. That makes it easier to recognize what state the latch is in.

Project 5-1 (Page 588) Using 4001 Gates. Be sure to change the pin numbers for the 7402 we are using.

Project 5-2 (Page 590) Using 4011 Gates. Be sure to change the pin numbers for the 7400 we are using.

