UCI MAE Walking Machines Class: Study Group 2021

Introduction to S-R Latches

How to eliminate switch bounce with the S-R flip-flop 7400 IC

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8-10-2021

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7400 NAND GATE USED FOR S-R LATCH (SET-RESET)

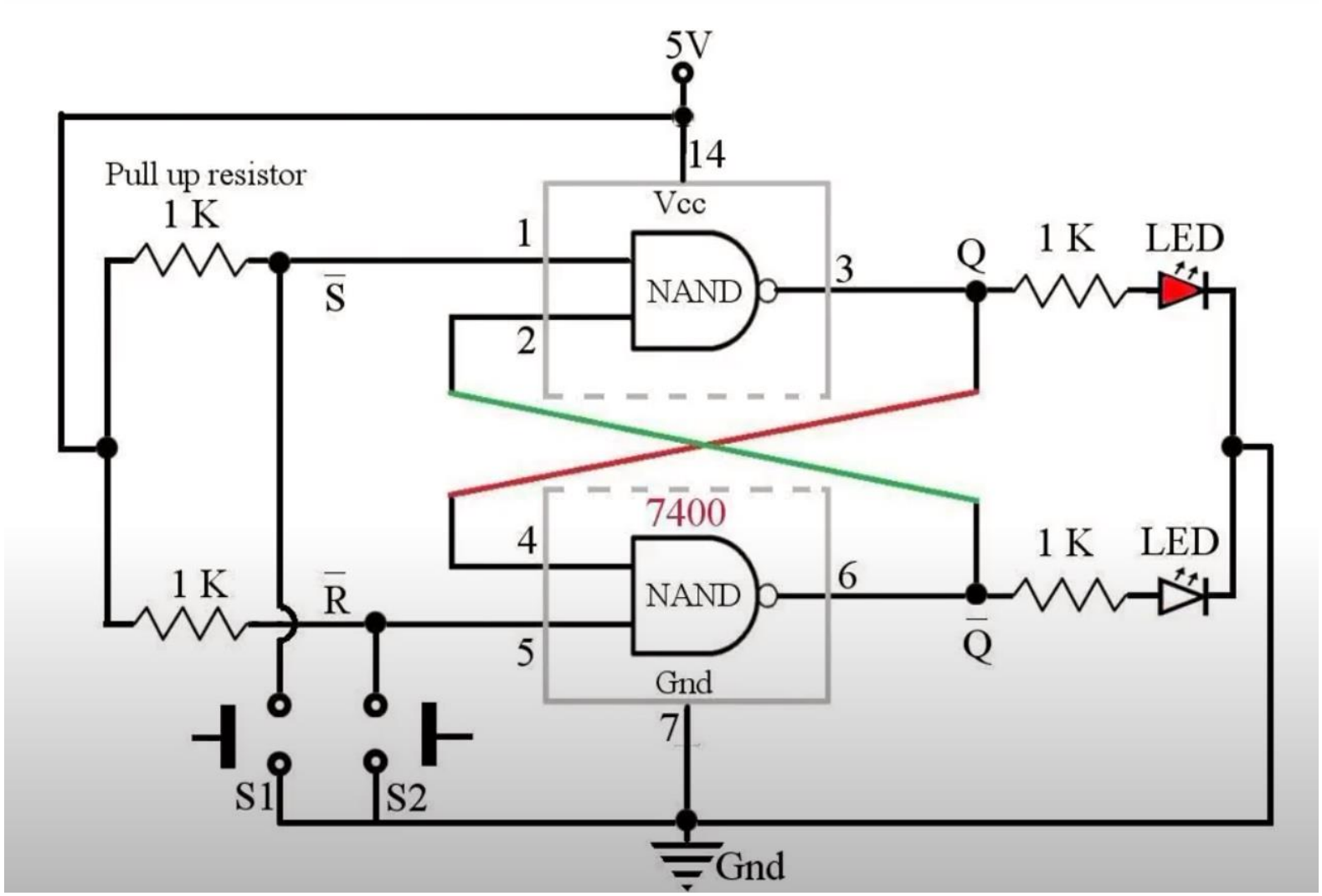

Figure 1: NAND S-R Latch with Push Buttons. From My Funny Electronics (2014)

S-R LATCH THEORY OF OPERATION

Debouncing an SPDT switch with an SR latch (Digi-Key)

"In the case of an SPDT switch, a common hardware debounce solution is to employ an SR latch. Ever since companies like IBM used this technique for the switch panels on their mainframe computers circa the 1960s, this approach has been regarded as the *crème de la crème* of simple hardware debounce solutions. Such a latch can be formed using two back-to-back two-input NAND gates; for example, by employing two channels of an SN74HC00DR quad two-input NAND IC from Texas Instruments (Figure 4).

When the switch's NC terminal is connected to ground, as shown in the upper half of Figure 2, this forces the output of gate g2 to logic 1. In turn, the two logic 1s on the inputs to gate g1 force its output to logic 0. By comparison, when the switch's NO terminal is connected to ground, as shown in the lower half of Figure 4, this forces the output of gate g1 to logic 1. In turn, the two logic 1s on the inputs to gate g2 force its output to logic 0.

The reason this circuit works so well is that when both of its inputs are in their inactive logic 1 states, the SR latch remembers its previous value. Remember that when an SPDT switch is toggled, whichever of its terminals is connected to ground—at that moment in time—bounces first. Since these bounces are between its original value (logic 0) and its new value (logic 1), they have no effect on the current state of the SR latch. It's only after this terminal ceases to bounce that its counterpart starts to bounce, at which time the SR latch changes its state. " (Maxfield, 2021).

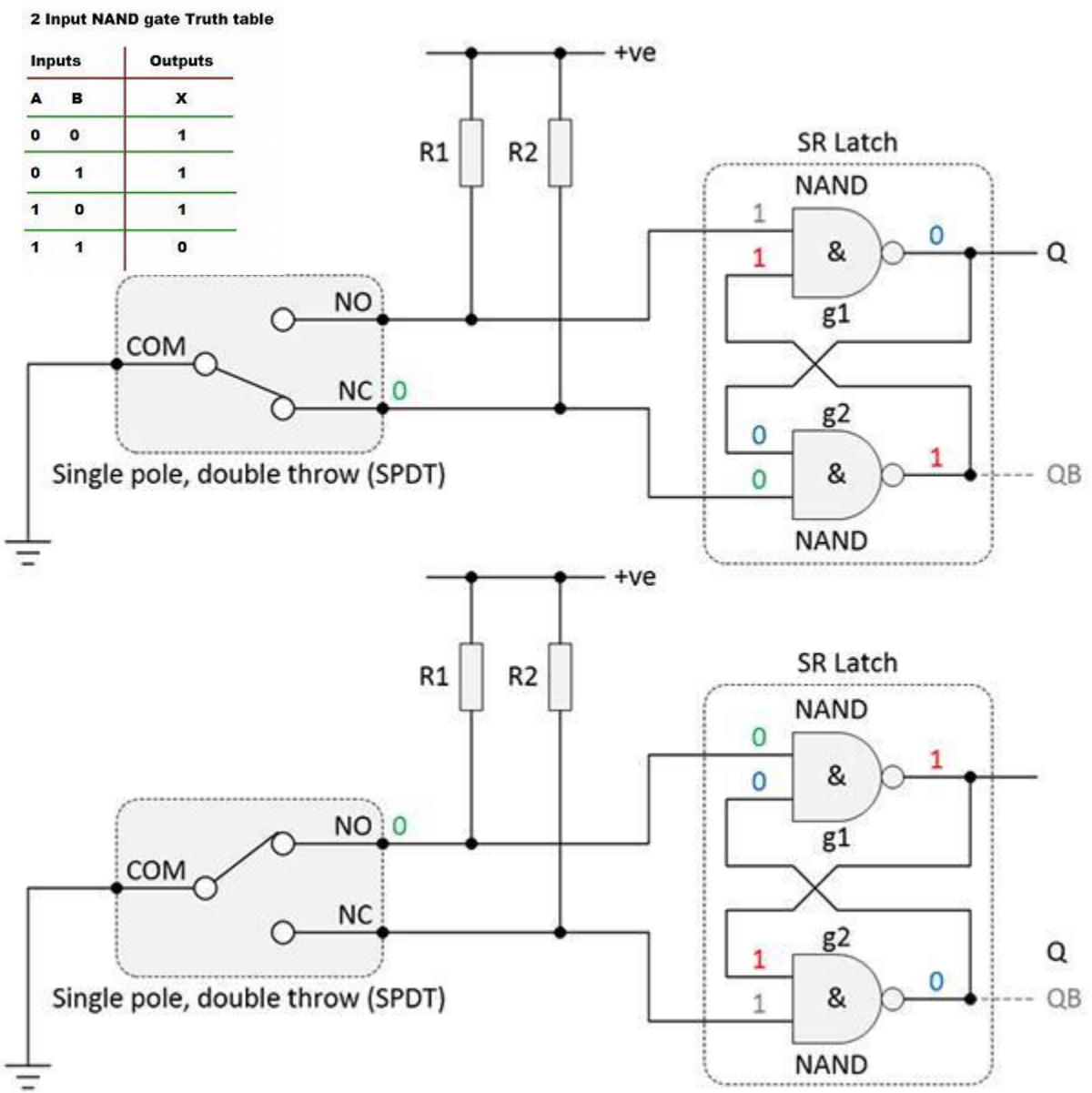

Figure 2: Top State shows RESET (R) Q=0 and Bottom shows SET state Q=1

SWITCH BOUNCE SETUP FOR DEMO

My micro switch (SPDT) connected to 5V via a 100K Ω resistor and scope connections.

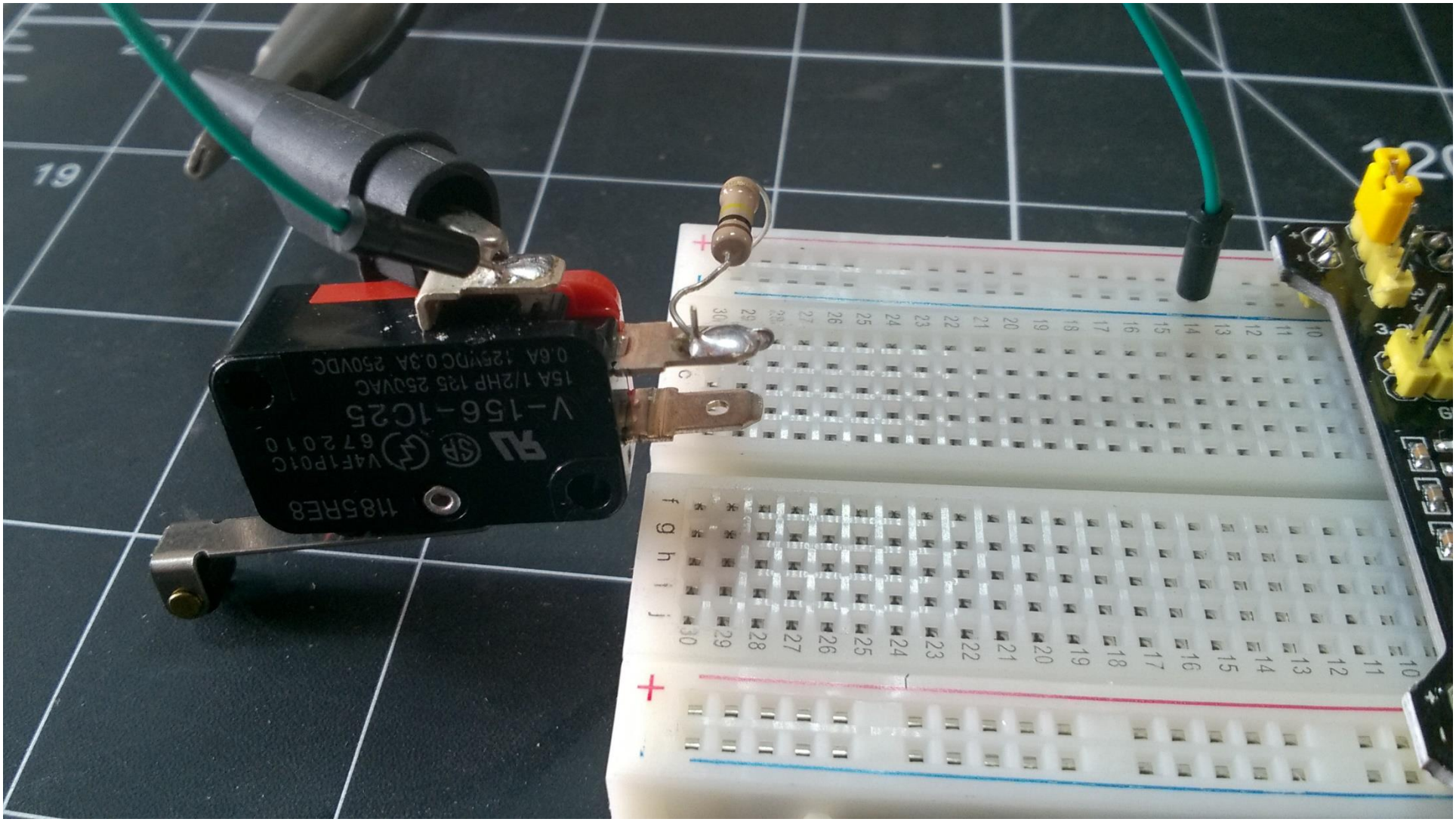

Figure 3: SPDT Micro switch with 100K Resistor and Scope Probes to Show Point Bounce

Here is a closer look at the scope setup. With the power turned on, I can press/release the switch and the point bounce can be seen on the scope.

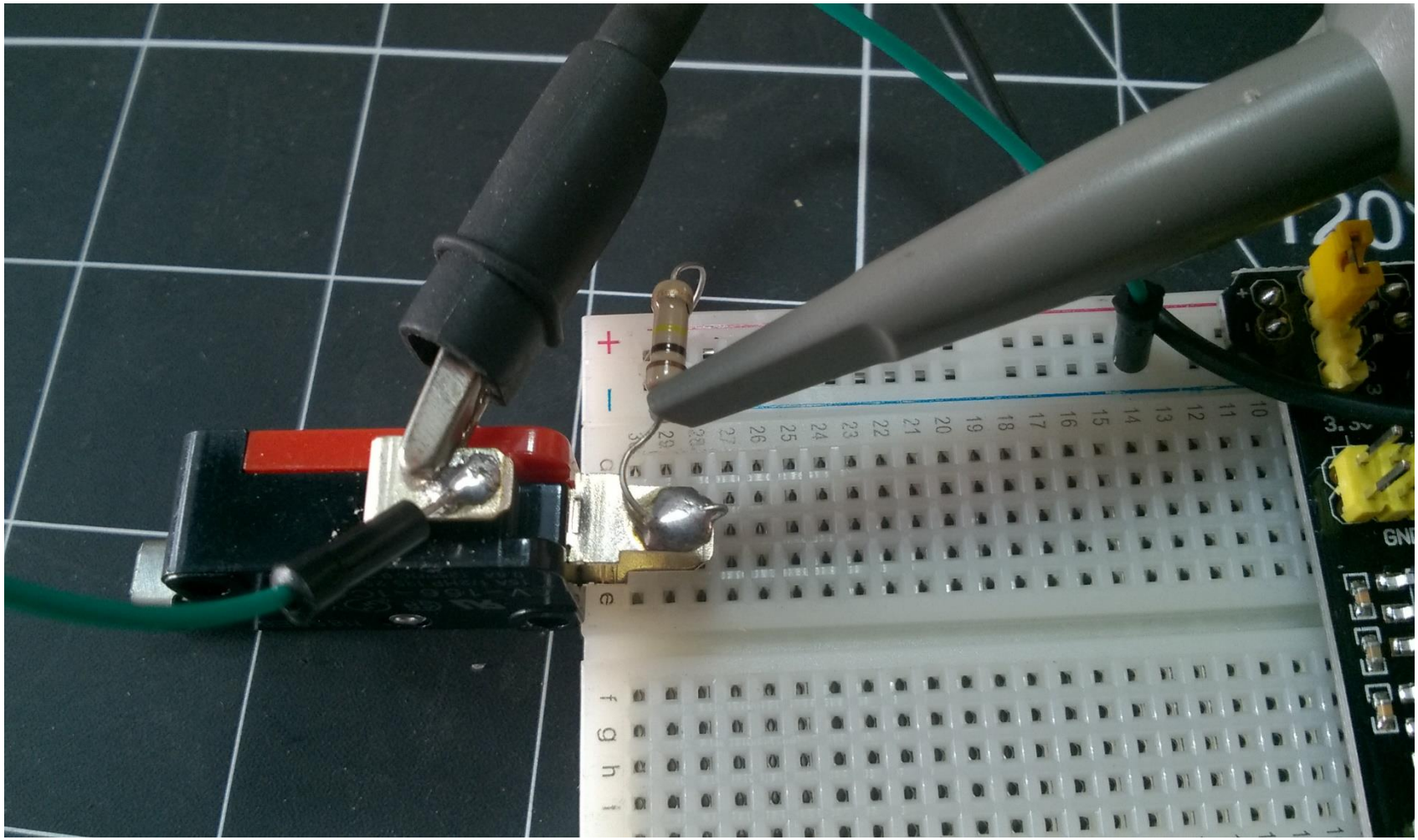

Figure 4: Close up View. Notice the scope probe is connected to the switch side of the resistor.

SETTING UP THE S-R LATCH DEMO

Use the 7400 NAND (Not AND) IC for this demo. Make sure to orient the chip with the notch to the left side of the breadboard.

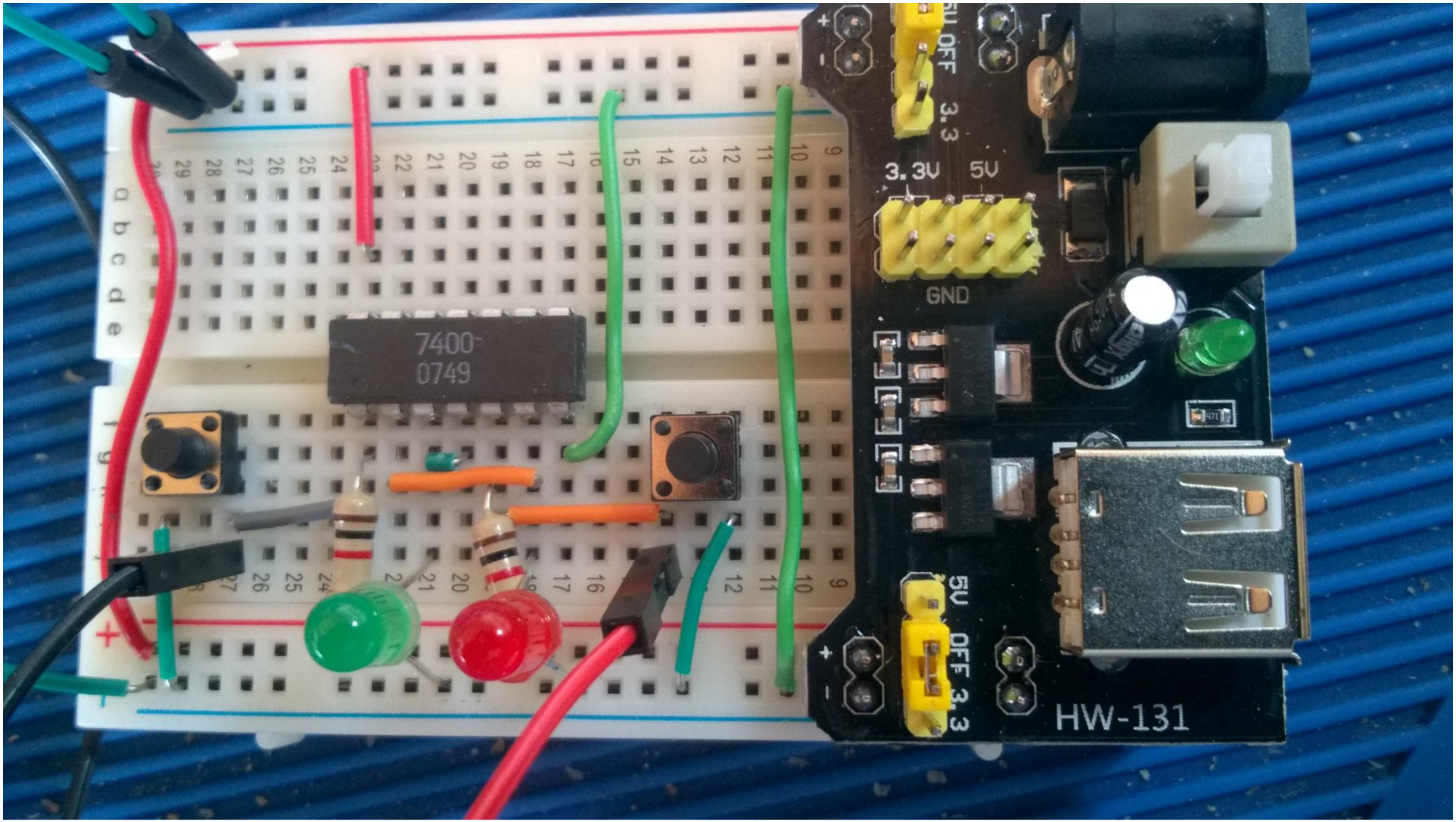

Figure 5: Top view of the 7400 NAND Gate demo

Here is a close-up view of the circuit.

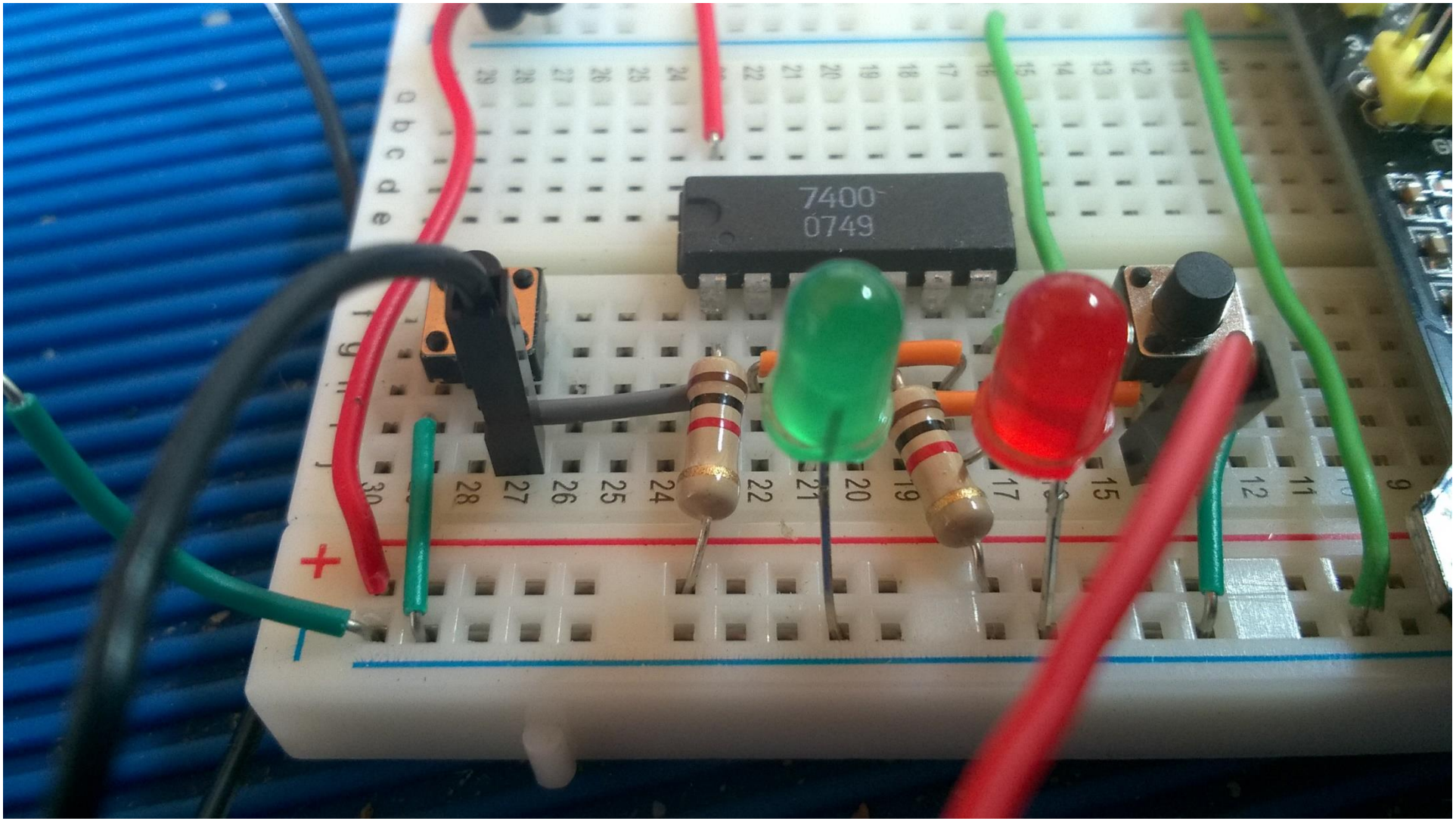

Figure 6: Close-up view of the 7400 latch demo

Here is the rear view of the circuit. Unless you have a micro switch, just use your push-button switches.

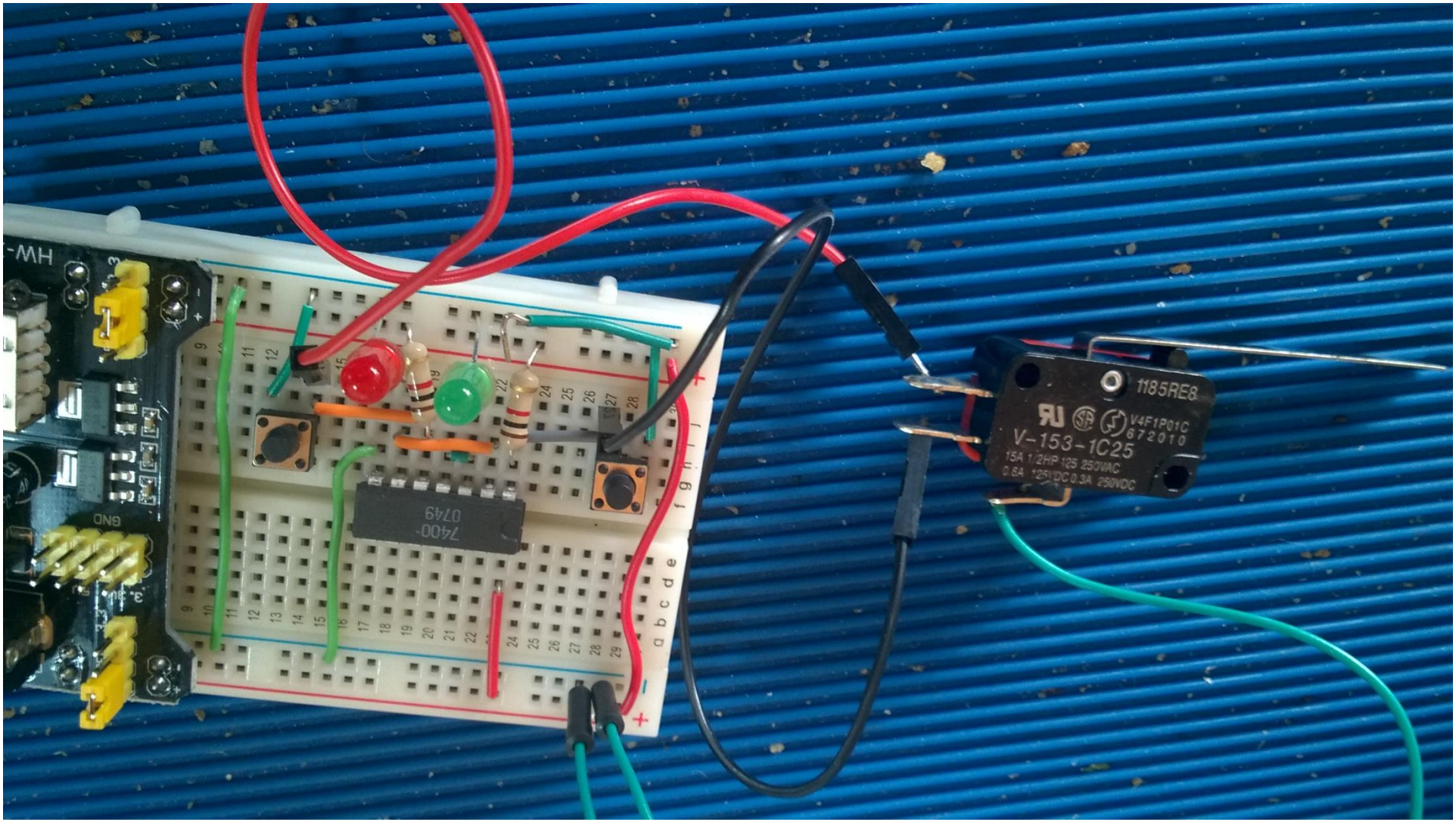

Figure 7: Rear view of the S-R latch circuit. The microswitch will be used to display images on the scope.

SWITCH DEBOUNCING CIRCUIT SCOPE TRACE

Figure 8 shows the effectiveness of the S-R latches ability to suppress switch bounce. The yellow trace measures the point bounce on the switch. The blue measures the OUTPUT/SET or Q pin on the 7400 IC (pin #3).

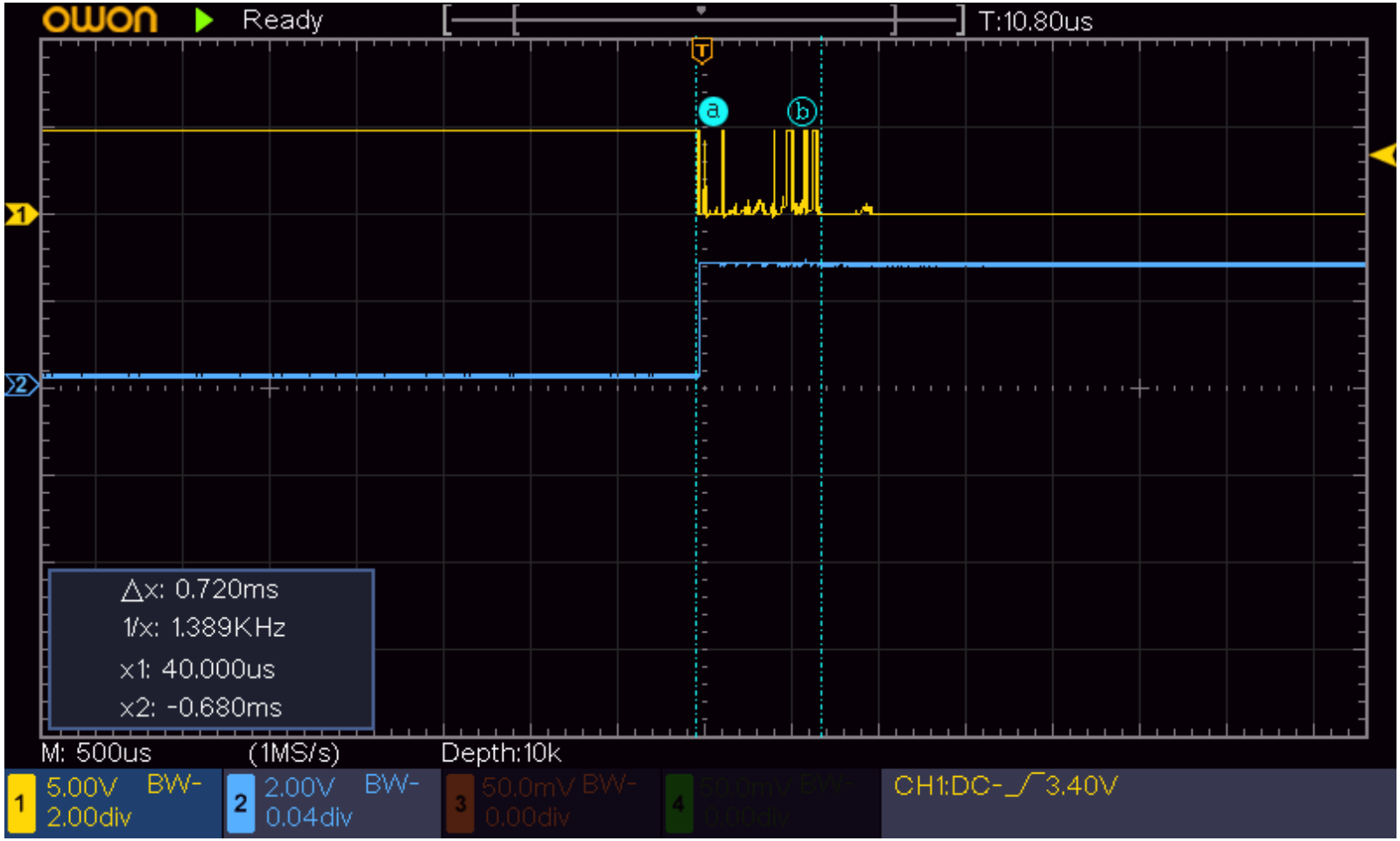

Figure 8: Scope image showing the effectiveness of the S-R latch.

REFERENCES

Maxfield, Clive (2021). *How to Implement Hardware Debounce for Switches and Relays When Software Debounce Isn't Appropriate*. Digi-Key Electronics, https://www.digikey.sg/en/articles/how-to-implement-hardware-debounce-for-switches-and-relays.

My Funny Electronics (2014). *Amazing Animation for Demonstrating S-R Latch*. Yoube.Com. https://www.youtube.com/watch?v=SQOcU0tGuFs.