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# Exploring the LM555 Timer Integrated Circuit

## BUILDING ASTABLE, BI-STABLE, AND ONE-SHOT TIMER CIRCUITS

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# CHAPTER 1

## WORKING WITH THE 555 TIMER IC

The 555 timers can be configured in thousands of ways. Here, we are going to look at the top three most popular circuits. These chips use analog components on the input but they output a digital signal/pulse at TTL logic levels. Recall that 0 - .4 volts = LOW and 2.4 – 5 volts = HIGH.

Note that unlike the Arduino®, the LM555 can source 200mA so it can be used to turn on a much larger load than a typical microcontroller. Recall that the 2N2222 can source 800mA so the 555 could drive a transistor when you need to drive lamps or relays, for example.

Mode 1: ASTABLE MODE**:** The IC can work as an oscillator. It can produce a square wave that can be used to blink an LED, for example. The output looks like the PWM signals we have worked with. The circuit on the far left blinks the green LED on and off at a rate of about 1 sec. The blink rate is determined by the values of a Resistor-Capacitor pair.

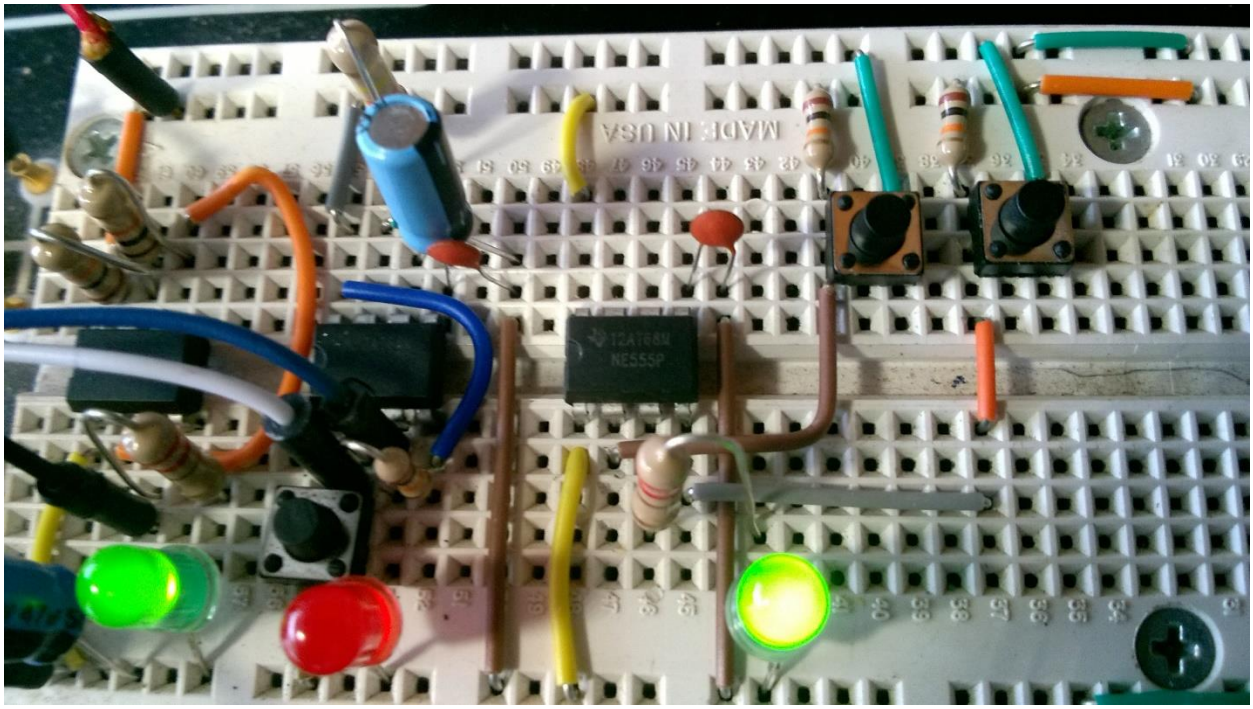



*Figure 1-1: Three LM555 timer circuits. Left: "Blinky", Center "Egg Timer", & Right "Flip-Flop"*

Figure 1-2 shows the circuit simulation in Multisim and transistor equivalent circuit. C1 charges via R1 and R3. When C1 is 1/3 charged the IC is triggered (Pin 2) and the LED turns on. Pin 4 monitors the voltage on C1 and when it reaches 2/3 of max charge it turns the output off (LOW).

C1 is discharged via R3 on pin 7 (discharge). Inside the IC there is a transistor that, when turned on, grounds pin 7 and that is how C1 discharges. When the voltage on C1 drops to 1/3 its capacity, pin 7 is turned off and the charge cycle repeats. **It is recommended that the control voltage pin#5 should always be sinked to ground via a .01uF ceramic capacitor to provide stable operation.**

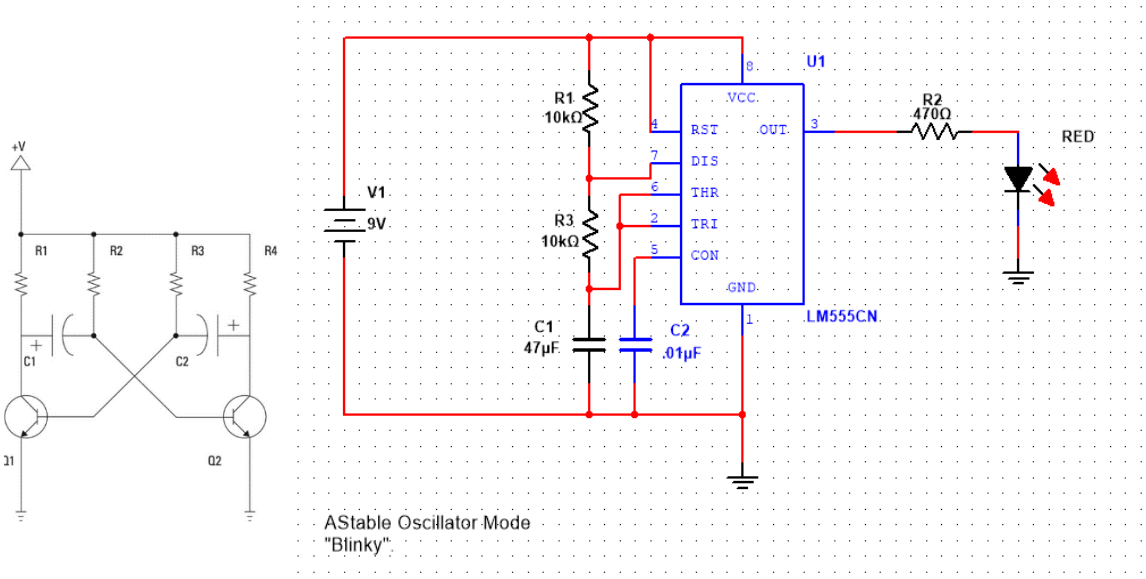



*Figure 1-2: Astable Mode. Transistor version on the left. On right, the combination of R1, R2, & C1 determine the blink rate of the LED.*

Now look at Figure 1-3. This shows the output signal on pin 3. Notice the duty cycle is > 50%. That is because the capacitor (C1) charges through BOTH R1 & R3 but only discharges through R3. So even though my resistors are both 10K, the “ON” time is twice that of the “OFF” time. We will look at an alternative circuit in a moment that will show how to get around this limitation.

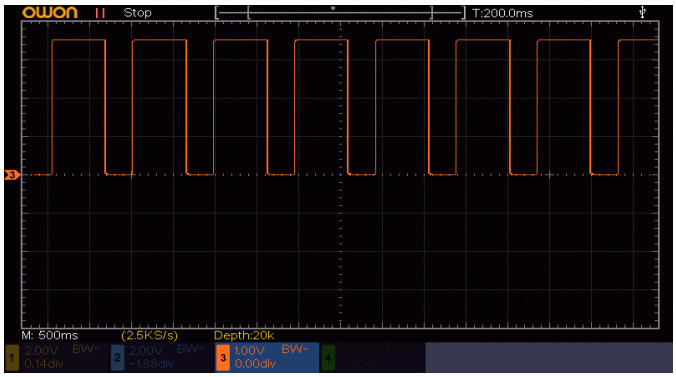



*Figure 1-3: Scope image of the output from LM555 in Astable mode.*

## Blinky Version 2

Now let's examine this variation of the original circuit. If you want the duty cycle of the timer to be 50%, then we need to make sure that the capacitor is charged and discharged through the same value resistor. Look at Figure 1-4**. Update: if you use a circuit running on Vcc=3.3V, use a Schottky diode instead. A 1N5817 will turn on/off faster and only needs ~3V to turn on. This will help you achieve a 50% duty cycle. This is especially true when we examine FPGA's (Field Programmable Gate Arrays).**

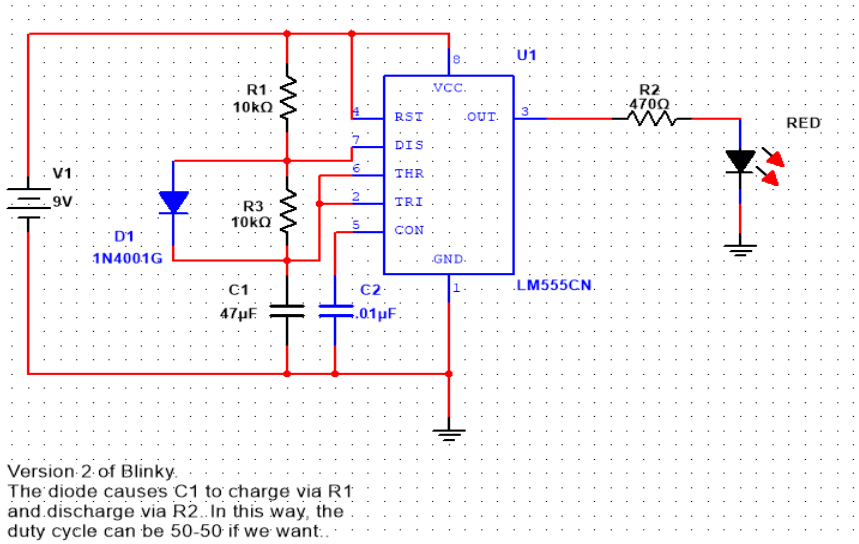



*Figure 1-4: This shows the "Blinky" circuit set up to run at a 50% duty cycle. The addition of D1 allows C1 to charge through R1 and discharge through R3. Since they are the same value, the duty cycle is 50%.*

I added a silicone diode across R3. When power is turned on, current flows through R1 to C1. R3 is taken out of the circuit by the conducting diode. If you use a diode, use these formulas:

$T_{Period}$ = .7 X (R1 +2R3) X C1
$T_{high}$ = .7 X R1 X C1
$T_{low}$ = .7 X R3 X C1

When the timer stops, C1 is discharged through R3 only because D1 is reversed biased. Thus, the "ON" and "OFF" periods will be the same (Figure 1-5).

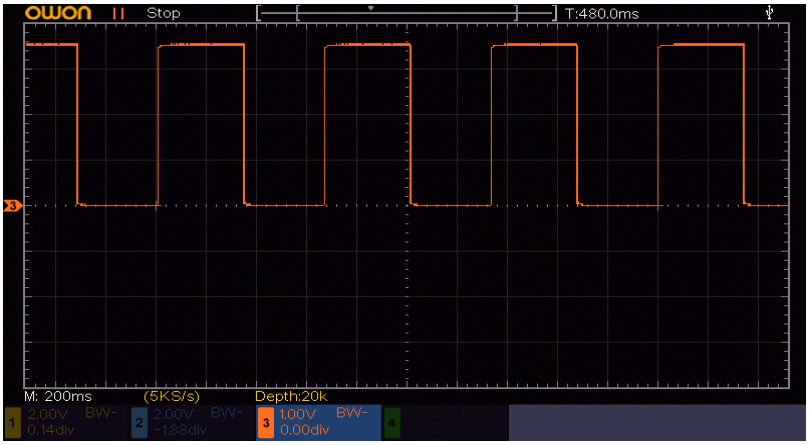
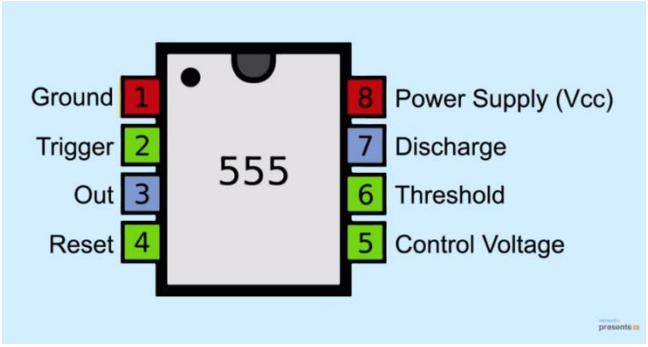



*Figure 1-5: With D1 in the circuit, the duty cycle is now 50%*

## HOW THE LM555 WORKS

To understand how the 555 works its magic, let's take a closer look inside of it. Perhaps a short explanation for the pins will help.




1. **GND** is tied to your circuit ground or B- side of a battery.
2. The **TRIGGER** on pin 2 starts the chip doing what you want. When the voltage on pin 2 equals 1/3 of the supply voltage, it starts the timing process. A normally open push button can be used to pull pin 2 to ground momentarily. This is called *Active Low triggering.* In Figure 2, this trigger voltage is controlled by the amount of charge on C1. So, without any software or programming, this chip goes about its business making square waves. The duty cycle can be changed by choosing different values for R1, R3, and C1. Pin 2 must be pulled up to B+ by a resistor (10K in my example).
3. The **OUTPUT** pin is the digital signal/pulse that drives the LED in my circuit. But it could be used as a "clock pulse" and connected to the input of an Arduino, for example.
4. **RESET** can be used to interrupt the timing process. It must be pulled LOW to activate it just like the trigger pin. So, like the trigger pin, a pullup resistor is used to hold it HIGH until the switch is depressed and forces it LOW momentarily.

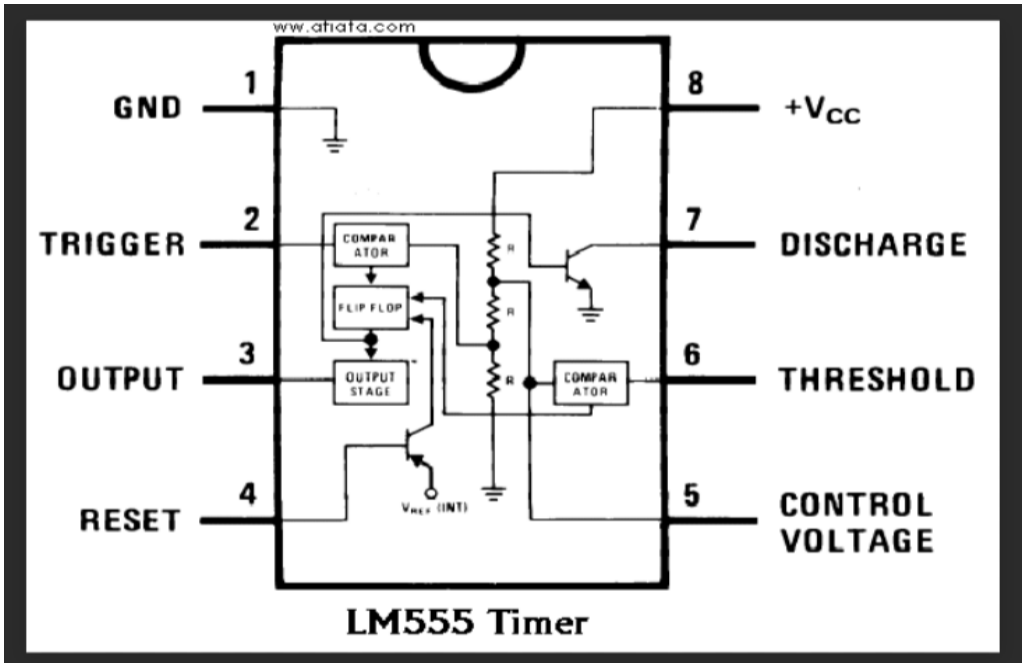



*Figure 1-6: Block diagram of the LM555 IC. Notice the Flip-flop and voltage comparators (OP-Amps).*

5. **CONTROL VOLTAGE** on pin 5 is seldom used. Normally, it is connected to ground via a .01uF ceramic capacitor. Sometimes, it is used to change the threshold voltage. In our circuits, it will be tied to ground through the capacitor.
6. **THRESHOLD** on pin 6 is used to monitor the voltage across C1 that is discharged by pin 7. When the charge on C1 is 2/3 of the B+ supply, the timing stops, and the output goes LOW.

7. **DISCHARGE** on pin 7 is used to discharge C1. Remember, C1 and R1 (in this example) determine the timing cycle. In most circuits, this pin is pulled HIGH through a resistor (R1 in my case) and to ground through C1. That way, it will go LOW or HIGH based on the voltage across C1. You can see the transistor circuit inside the 555 that can pull pin 7 low to discharge C1.
8. **VCC B+** on pin 8 supplies power to the chip (4.5 – 15VDC).

## Mode 2: MONOSTABLE OPERATION

Monostable mode is often called "One-Shot" mode. Here, the 555 acts like an egg timer. Monostable just means the only steady state of the circuit is when it is at rest and the output is LOW. The circuit in the middle of Figure 1 shows this in action. I use one push-button to momentarily ground pin 2 (Threshold) and this starts the timer. At this moment, the OUTPUT goes HIGH. It remains high until the time interval has passed. Then, the output goes LOW again, and it waits for another trigger pulse.

The time interval can be calculated by a simple formula. The values of C1 and R1 make up what is called an R-C time constant.

$T_{seconds} = 1.1 \text{ X } R_{ohms} \text{ X } C_{farads}$

Example

Suppose we use R1 = 500KΩ and C1 = 10uF.

T = 1.1 X 500,000Ω X 0.00001F

T = 5.5 Seconds.

This means that when I push S1 momentarily, the timer starts, and the LED turns on. After ~5.5 seconds or so, the timer stops, and the LED goes off.

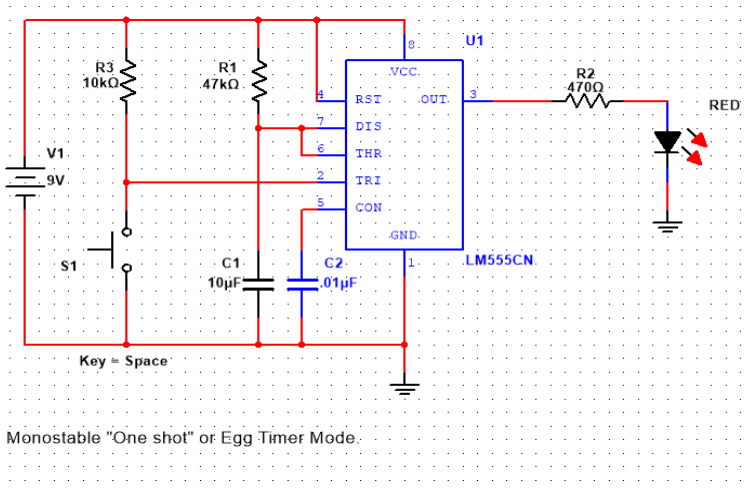



*Figure 1-7: Here is the "Egg-Timer" circuit in Multisim. When S1 is depressed, the trigger is pulled LOW, and the timing cycle starts.*

In Figure 1-8, you can see the effect of momentarily depressing S1. The normally HIGH trigger line is pulled LOW for an instant and this turns on the timing circuits.

The output (blue trace) goes from LOW to HIGH and stays high until the timer turns off. Then it goes LOW again. Remember the R-C time constant determines the width of the output pulse.

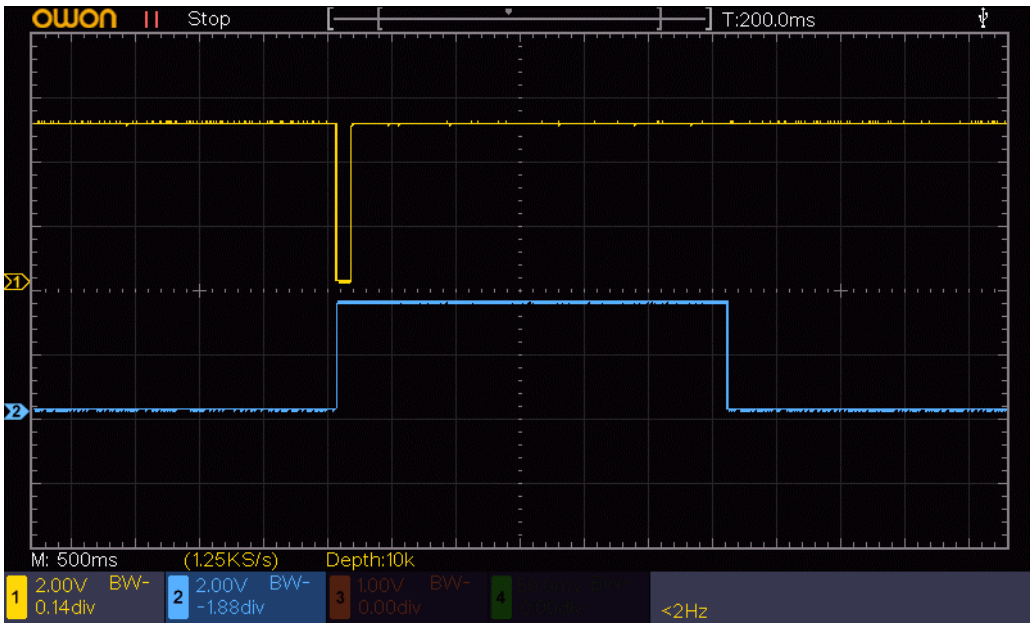



*Figure 1-8: Timing image for "Egg Timer". The yellow trace shows the trigger and the blue trace shows the output. When the trigger goes LOW, the output goes HIGH for ~5.5 seconds.*

Now look at this scope image. In Figure 1-9, the top, orange, trace is the astable mode output signal. The yellow trace is the trigger, and the blue trace is the output. Notice how the trigger goes low momentarily and the output stays HIGH for the length of the time constant. The green trace shows the capacitor charging. When the voltage across the timing capacitor reaches 2/3 of the supply voltage, the timing circuit inside the 555 stops and the output (blue) goes LOW and the capacitor is discharged (green trace) through the internal circuits in the timer chip itself. The 555 uses an internal transistor to open and close a path to ground for the capacitor to either be charged or discharged. This is done automatically. No other external components are needed.

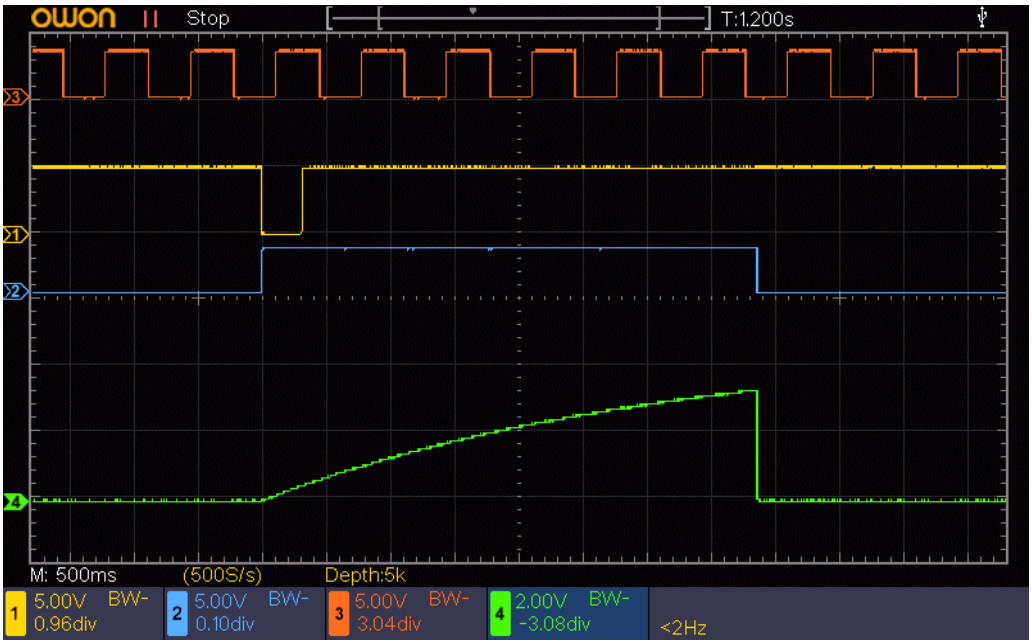



*Figure 1-9: LM555 timing diagram showing the Astable & Monostable modes.*

The power supply to the IC is 5V. I wanted to verify the voltage across the capacitor. The IC stops the timing when C1 charges to 2/3 of 5 or 3.3V. When I measured the amplitude of the charging capacitor (green trace), it was 3.2V when the timing cycle stopped, and the output went low.

You can see how fast the capacitor is discharged. That is because the transistor is connected to ground with very little resistance.

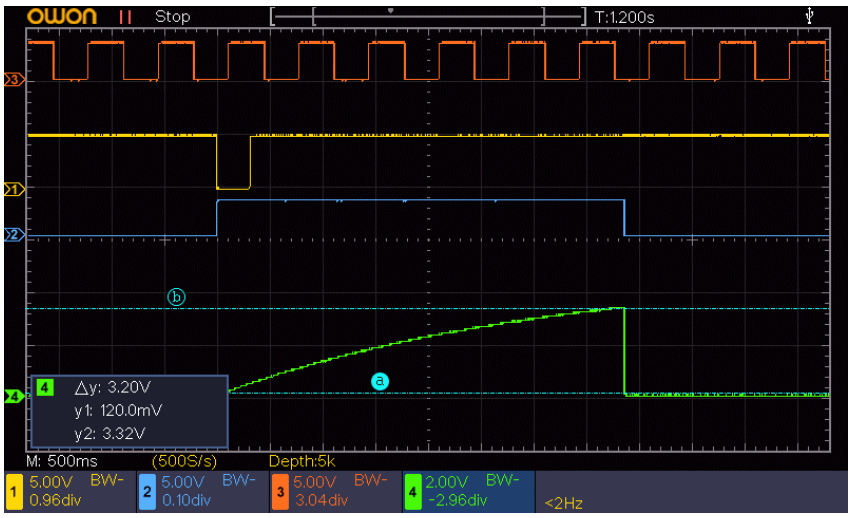



*Figure 1-10: Measurement of the capacitor charging. When it reaches 2/3 of the 5V supply, the timing is stopped.*

## Mode 3: BISTABLE OPERATION (FLIP-FLOP) MODE

We now come to the last example of my 555 configuration examples. If you refer back to Figure 1, you can see this circuit on the breadboard in the middle of the image where the green LED is on. This mode uses a S-R flip-flop or latch inside of the 555 itself. Keep in mind that in fast computers and other devices, the 555 is not used for this purpose I am describing here. A latch or flip-flop must be able to change states very quickly and the 555 cannot compete with the high-speed logic gates. But it could sure be useful with DIY and hobbyist projects.

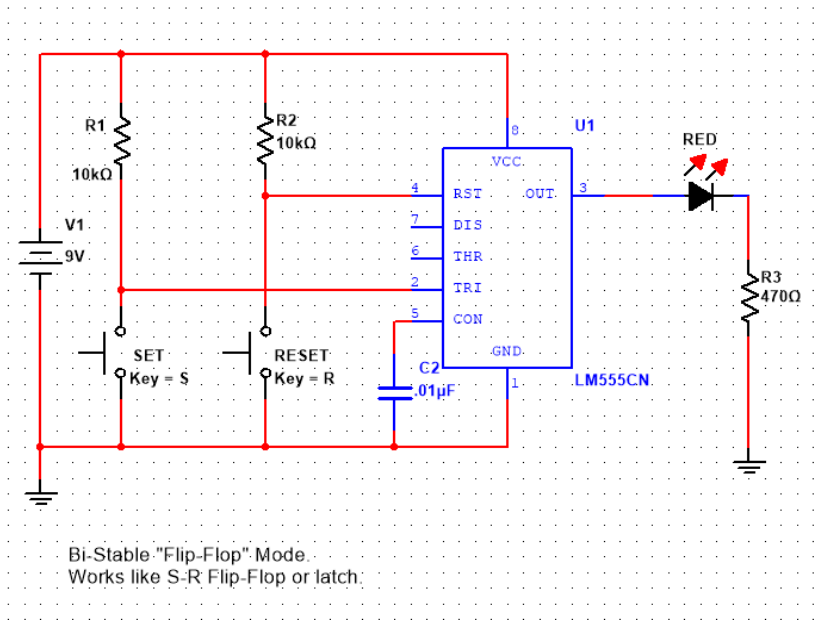



*Figure 1-111: LM555 configured as a Flip-Flop/Latch*

The schematic in Figure 1-11 shows how I used two switches to control the latch. We have a SET and RESET button just as we used with our NAND gate S-R latch examples in previous lessons. This circuit requires fewer components. Notice there is no capacitor because we aren't using any timing functions. We want to just set it and reset it.

Since the trigger (pin 2) is activated by a low signal or pulse (called Active LOW), it is pulled HIGH through R1 while at rest. The reset (pin 4) is pulled HIGH through R2 for the same reason. C2 is used to suppress any noise spike as the IC is triggered as in previous examples.

## Scope Images of the LM555 in Bi-Stable Mode

Now let's see how well the latch works in the 555. The top trace (red) in Figure 1-12 was captured when I pressed the SET button. As the trigger goes LOW, the output that drives the LED goes HIGH. It remains high until I press the RESET button. When the output is high, it supplies power to the LED and it lights up. This is called ***sourcing*** because the IC supplies a path to Vcc when activated.

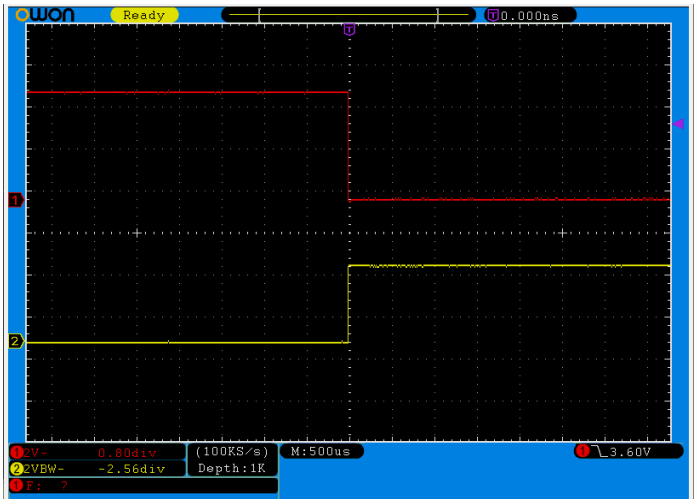



*Figure 1-12: Scope image of trigger (red) going LOW and output*

In Figure 1-13, the top trace shows the result of pressing the SET several times. You can see that once the latch is set, it ignores any further trigger pulses until it is first reset.

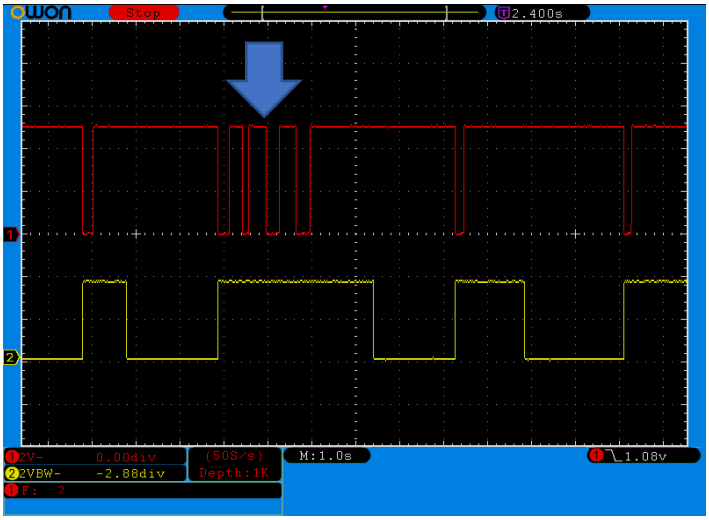



*Figure 1-13:This shows how multiple triggering has no effect once the latch is set.*

Don’t forget, that the manual switches create noise spikes when pressed. But as we saw in the NAND Gate latch demo (lesson 8), the output was very clean and free of noise. Figure 1-14 shows the typical point bounce (red trace) from the push buttons but the output (yellow) of the latch in our 555 is steady.

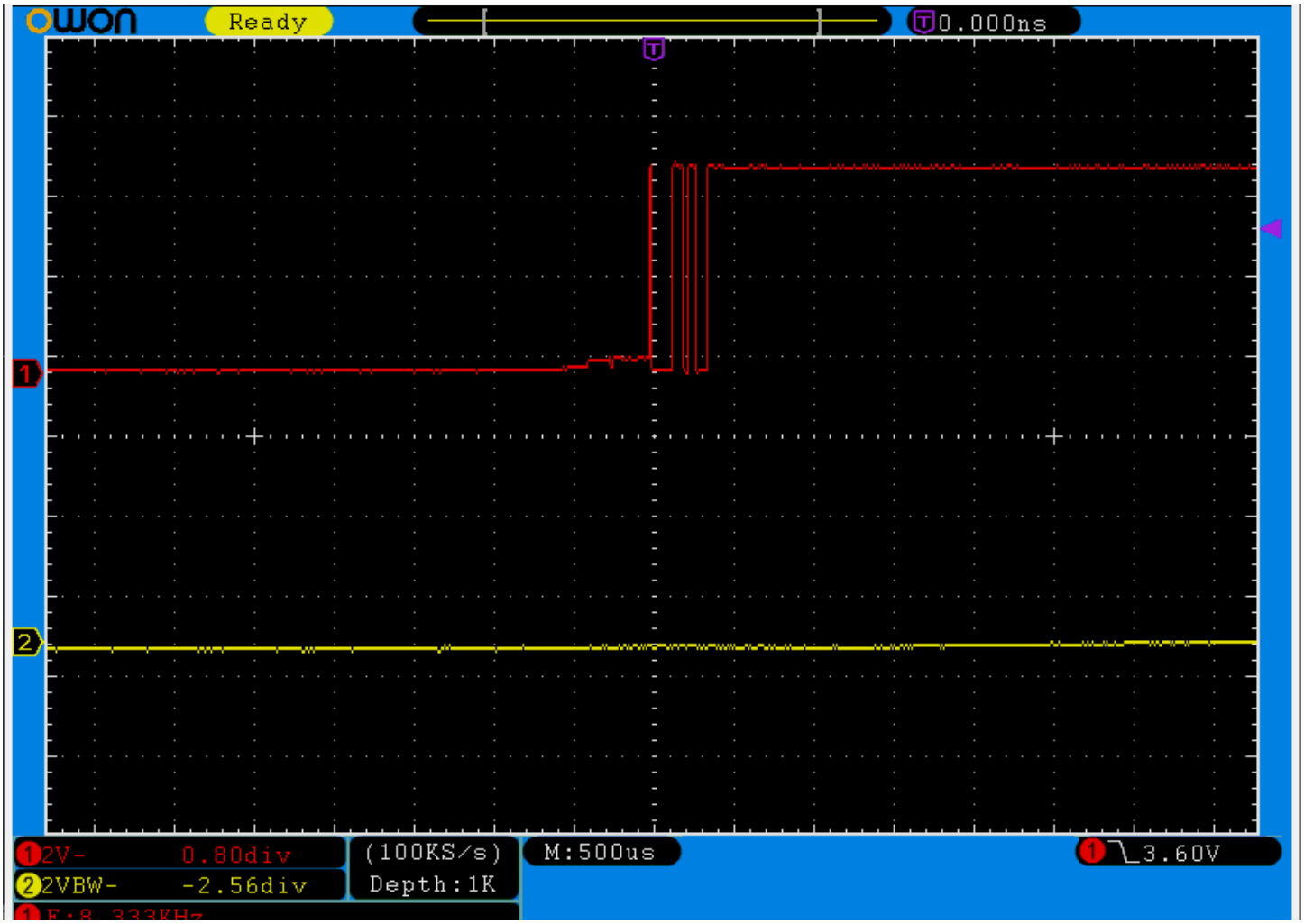



*Figure 1-14: Here the switch bounce is evident on the trigger pin but the output is unaffected.*

## BUILDING THE MONOSTABLE CIRCUIT

The circuit is shown below. I used two push-buttons, 220Ω resistor, LED, and .01µF ceramic capacitor (#103).

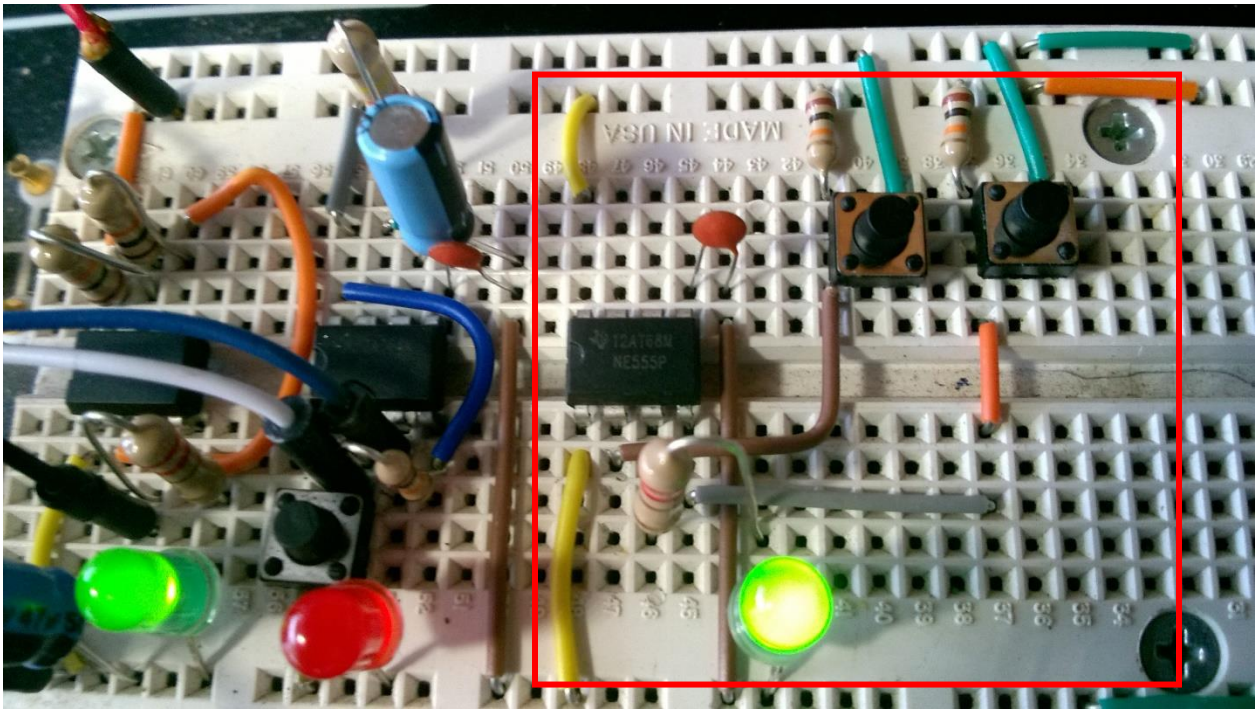



*Figure 1-15: Top view of the flip-flop circuit*

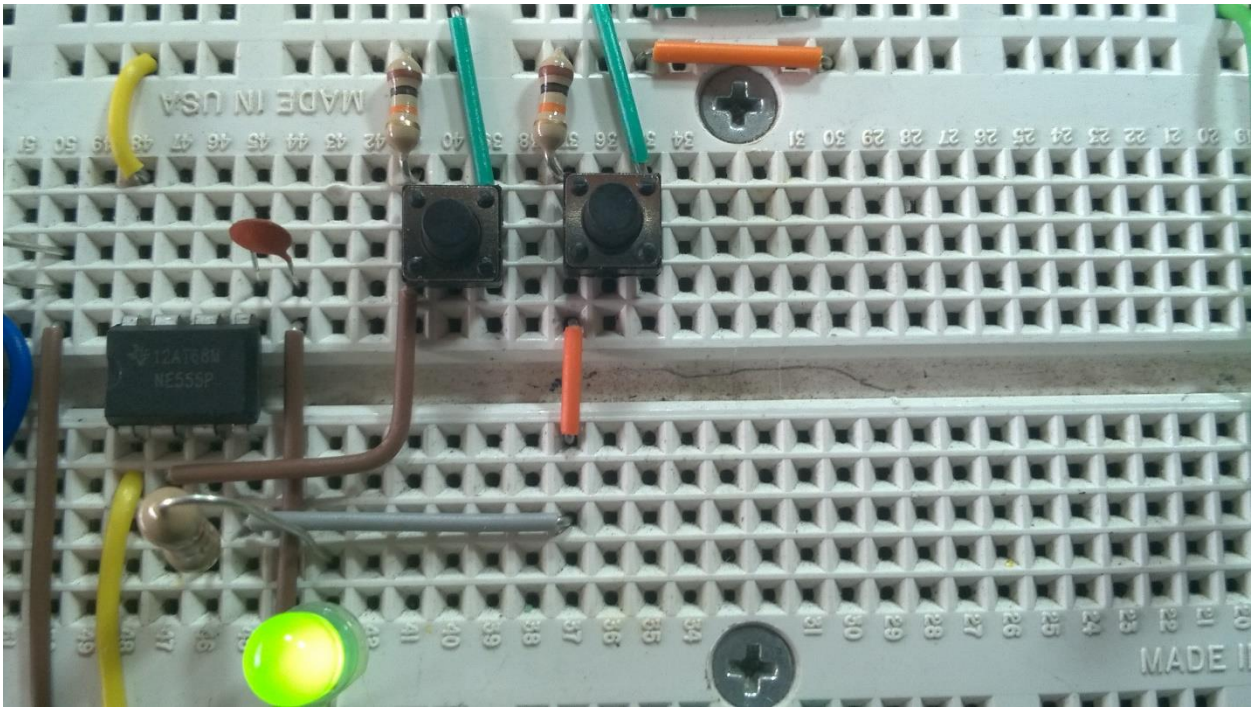



*Figure 1-16: Close-up view*

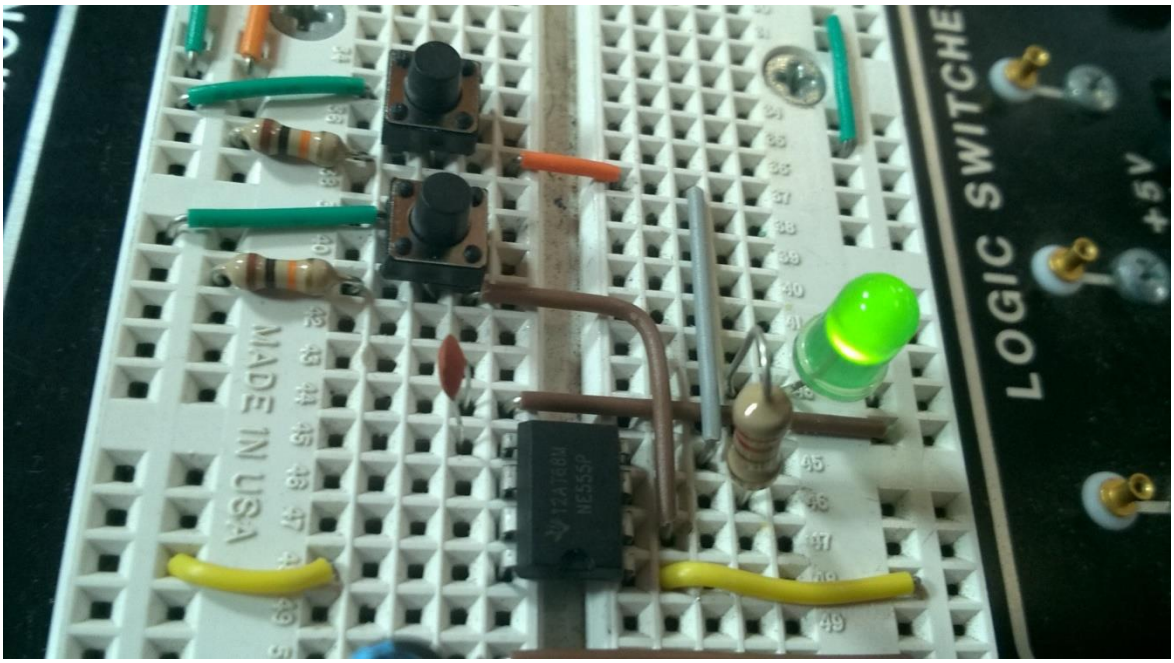



*Figure 1-17: Side view*

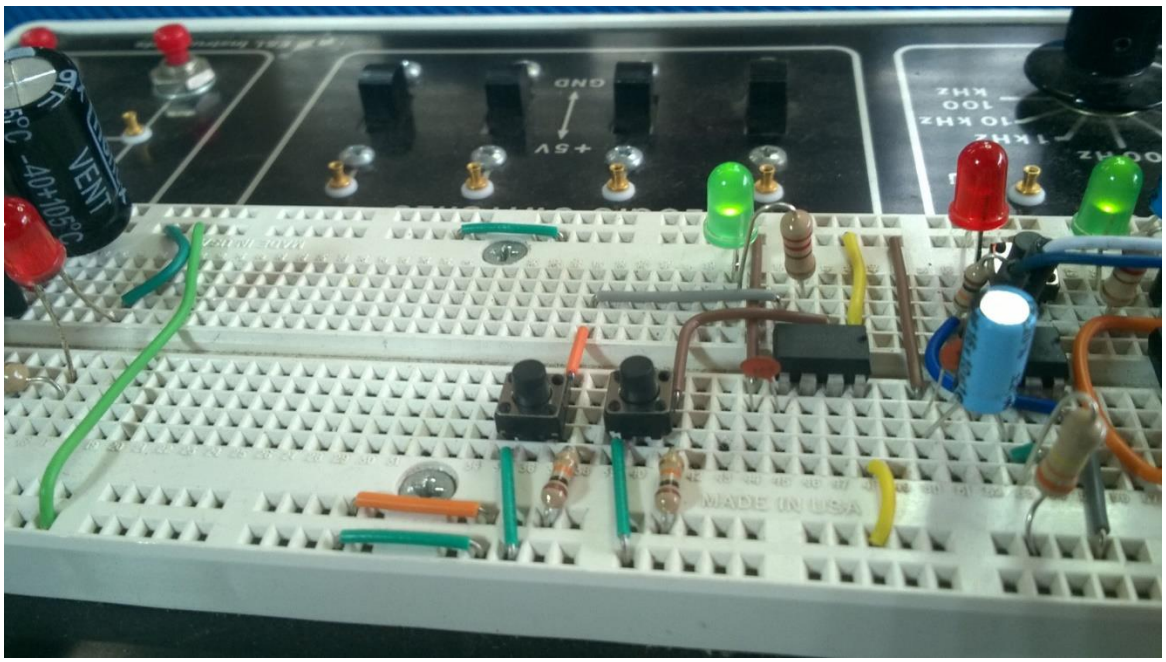
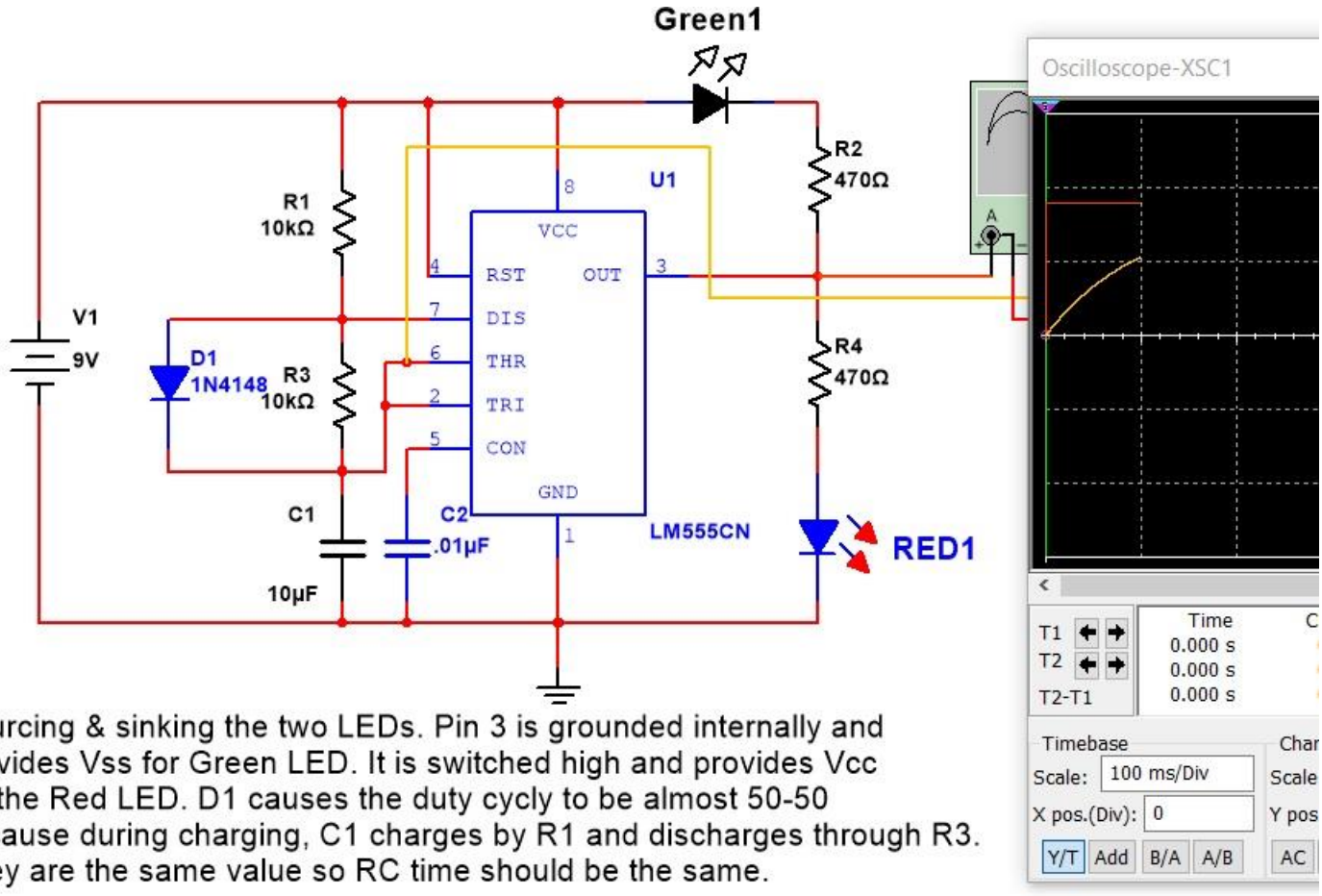



*Figure 1-18: Front view*

## Custom Circuit: Red-Green Flasher

Before we explore the inner workings of the 555, I wanted to show you how to combine some of its features into a custom application. The purpose of this example is to demonstrate how the IC can be used as a "Railroad Crossing signal". The 555 is configured to alternately flash two LEDs. I used a red and a green one here.

The main purpose of this demo is to show how *Sourcing* and *Sinking* work. I touched on this earlier. Sourcing refers to a circuit that provides a path to Vcc while sinking means the path is provided to ground. I want to show you how to 555 can do both, automatically without any software.




Sourcing & sinking the two LEDs. Pin 3 is grounded internally and provides Vss for Green LED. It is switched high and provides Vcc for the Red LED. D1 causes the duty cycly to be almost 50-50 because during charging, C1 charges by R1 and discharges through R3. They are the same value so RC time should be the same.

*Figure: 1-19 As C1 charges, pin 3 is HIGH and provides Vcc for the Red LED called Sourcing.*

In Figure 1-20, when the capacitor reaches 2/3 of its charge the 555 flips state and the output goes LOW. Pin 3 is connected to an NPN transistor inside the IC. When turned on, this transistor pulls pin 3 LOW. This provides a *ground* for the Green LED and it now lights up. This is the *sinking* phase of the cycle. When C1 is discharged to down to 1/3 of its voltage, the cycle begins again. Pin 3 goes HIGH and provides source (Vcc) to the Red LED and now it lights up. The frequency of this flasher is determined by the R-C time constant of C1 and R1 (charging) and C1 and R3 (discharging)

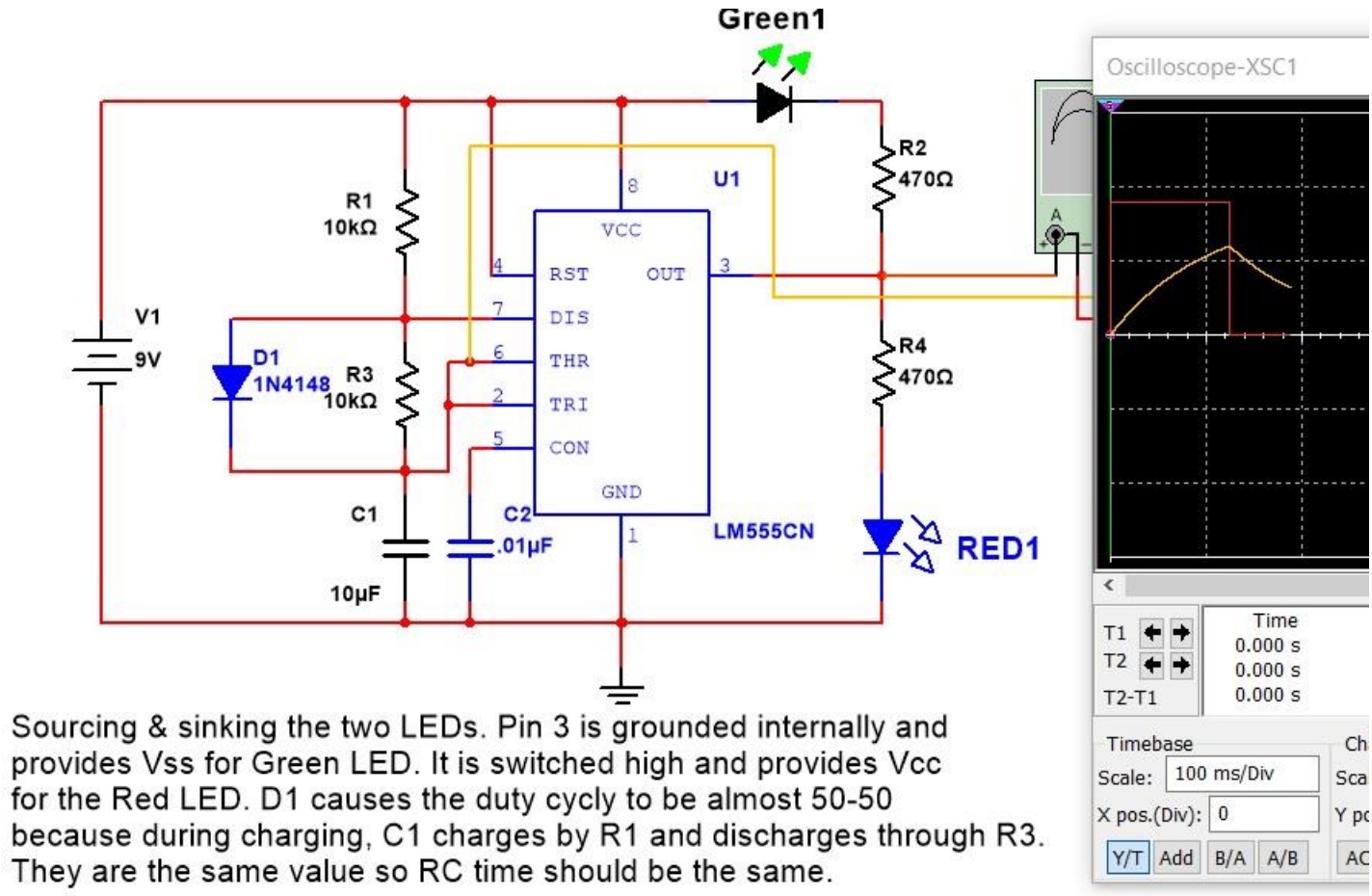



*Figure: 1-20 When C1 reaches 2/3 of its charge, the output goes LOW and the transistor inside the 555 provides a path to ground called sinking.*

# CHAPTER 2

## THEORY OF OPERATION

Now that we have figured out how to use the timer, let's take a deeper look into what makes it tick! The IC contains two transistors, two comparators, a flip-flop, an output circuit, and a voltage divider.

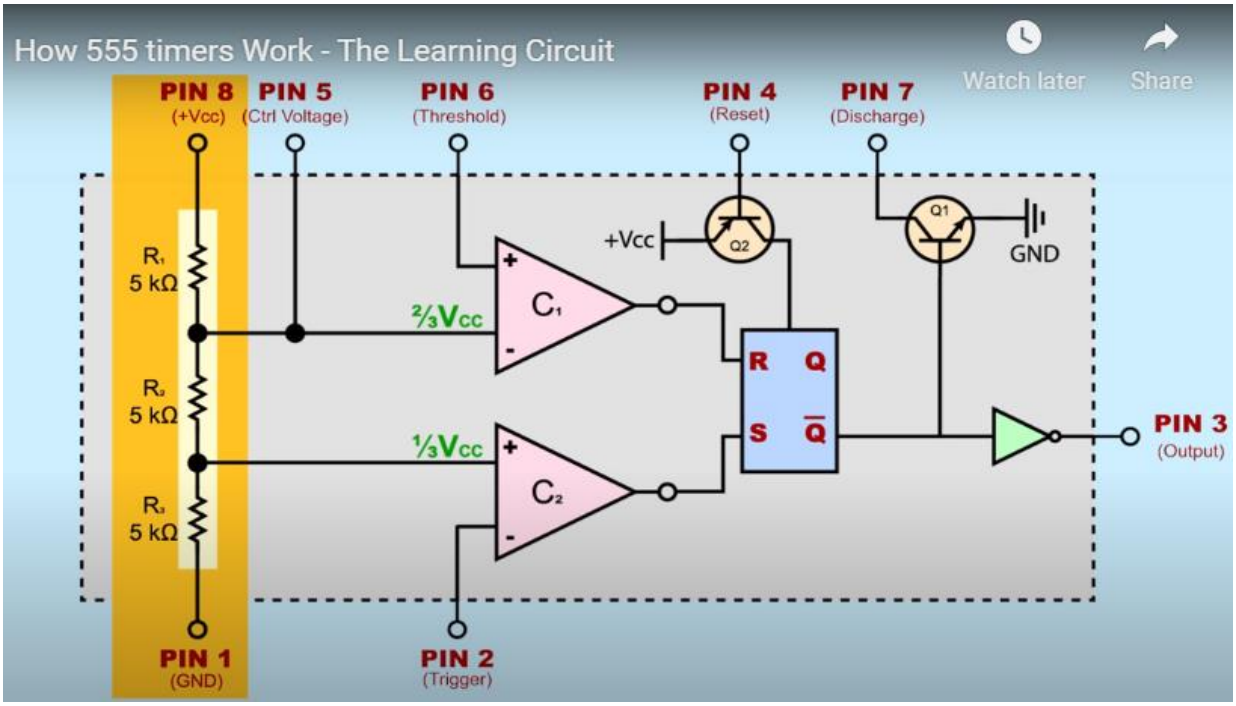



*Figure 2-1: Block diagram of the 555.*

### Voltage Divider

Let's look at the voltage divider first. You will notice there are three 5K resistors. Some people say this is where the chip got its name. But according to the designer, it was not the reason. Also, in many versions of the 555, 4.7K resistors are used. But the actual value does not matter as long as they are all the same.

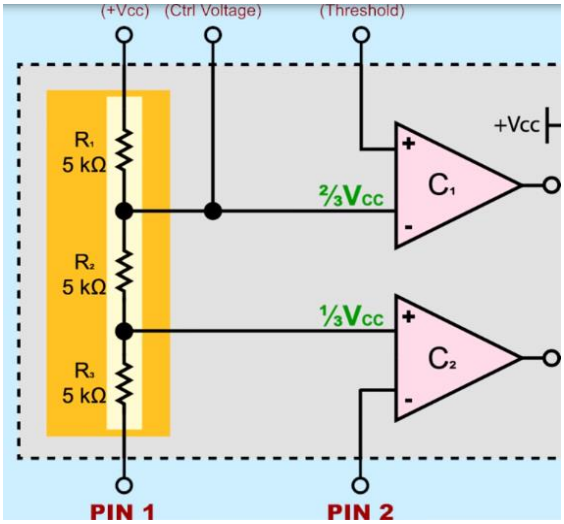



*Figure 2-2: Voltage divider circuit.*

According to the datasheet, the 555 can operate between 5-16VDC. Recall from the modes of operation section at the beginning of this paper, it is common to use the IC in *monostable* mode so that the comparators (pink triangle in Figure 2-2) can be used to create a square wave output signal.

This requires the external capacitor to be charged and discharged in a consistent manner. To make the chip function over a wide range of Vcc power, the voltage divider is used. The chip needs to be able to know when the external capacitor is 1/3 charged, and 2/3 charged regardless of the Vcc voltage.

## Comparators

We learned about voltage dividers earlier in this lesson. You may recall that when three equal value resistors are wired in series, the Vcc can be broken down into thirds. These two voltages serve as *reference voltages* for the comparators. The comparators need to measure the charge on the capacitor. They can't do that without something to compare to. Hence, the reference voltage from the divider solves the problem. Please keep in mind, the exact voltage on the capacitor is not of interest. We are only concerned about the ratio of the charge with respect to Vcc.

Let's look at an example. Refer to Figure 2-3 for this discussion. Suppose you use a 9V battery to power the chip. Since the voltage divider gives us 1/3 and 2/3 of Vcc, the first comparator ($C_1$) will get 6V at its minus (-) input and the second comparator (C2) receives 3V on its plus (+) pin.

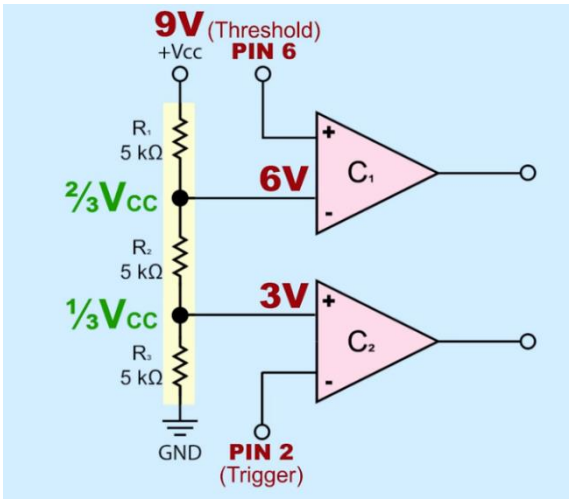



*Figure 2-3: Reference voltages applied to the comparator ICs from the voltage divider when Vcc = 9V.*

You see, when the voltage on the + pin of a comparator is greater than the voltage on the minus (-) pin, the output of the comparator is HIGH. Otherwise, it is LOW. So these comparators act like a hybrid device. That is, they can take analog inputs and produce a coresponding digital output.

Also notice, the *Threshold* pin connects internally to the "+" pin of $C_1$ and the *Trigger* pin connects internally to the "-" pin of $C_2$. As long as the threshold of $C_1$ < 6V, the output is LOW. If the voltage at pin 6 > 6v, the output will switch to HIGH.

Now consider $C_2$. If the *Trigger* is < 3V, the output is HIGH. If pin 2 were to be larger than 3V, the output would go LOW (Figure 2-5). So the simple rule is when the "+" pin is greater, the output is "+" or HIGH. When the "-" pin is greater the output is "-" or LOW.

Try to keep in mind, this relationship of the trigger and threshold is used to determine the capacitor's charge. The ouputs of the comparators feed the S-R Flip-Flop as we will see next.

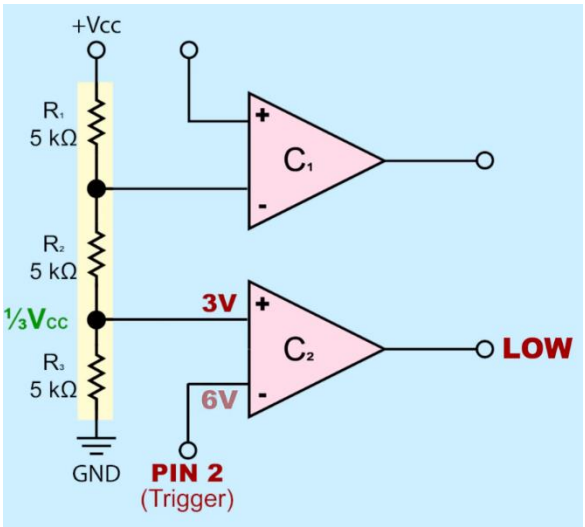



*Figure2-4: The bottom comparator receives 1/3 of Vcc and is connected to the trigger. If the trigger exceeds 3V, the output goes LOW, otherwise it goes HIGH.*

## S-R Flip-Flop

Figure 2-5 shows the comparators and S-R latch section. The output of the top comparator feeds the RESET of our flip-flop while the bottom one feeds the SET input. In the actual 555, only the $\overline{Q}$ output is used. This is connected to the output pin #3 and a couple of transistors and a buffer that inverts the 555 output.

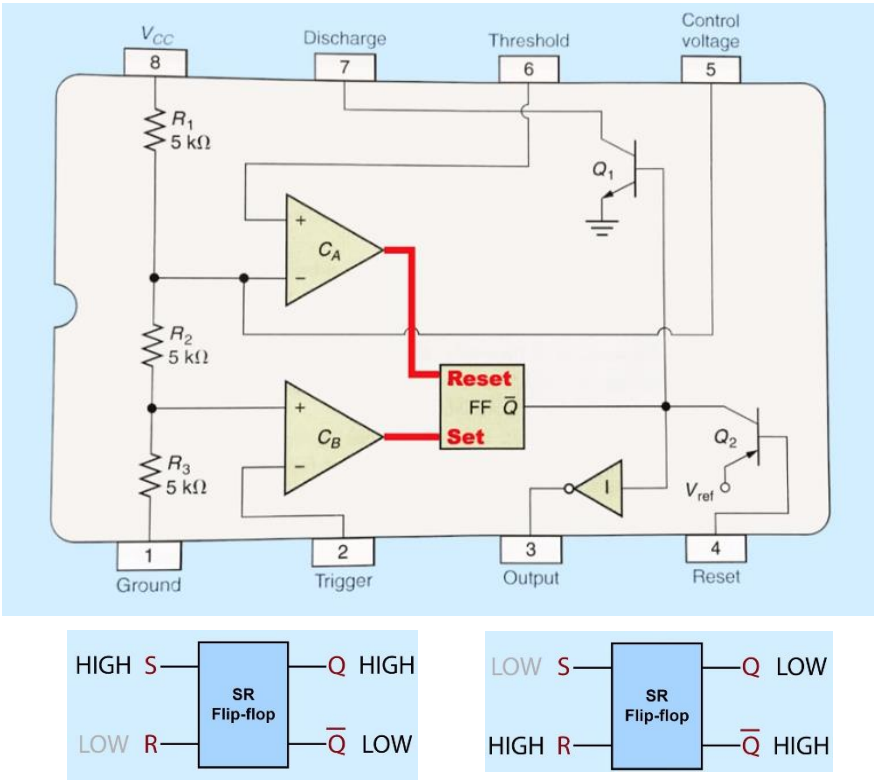



*Figure 2-5: The comparators feed the S-R Flip-Flop inputs.*

Let's take a look at the whole process up to this point. We need to understand how the voltage divider, comparators, and the flip-flop work together.

## Analog to Digital Processing

Refer to Figure 2-6. Since Vcc = 9V, our voltage divider supplies 6V to the top comparator as a reference. When the capacitor is charging, the voltage at pin 6 is less than 6V so the output of the comparator is LOW. When the "+" is greater than 6V the comparator goes HIGH. Otherwise, it is LOW as we see here. This causes $\overline{Q}$ to go low. But wait, I thought when the Flip-Flop went HIGH it turned something on? It does. The output signal gets inverted by the little triangle symbol marked "I" in Figure 2-6. The "I" stands for inverter. Hold that thought!

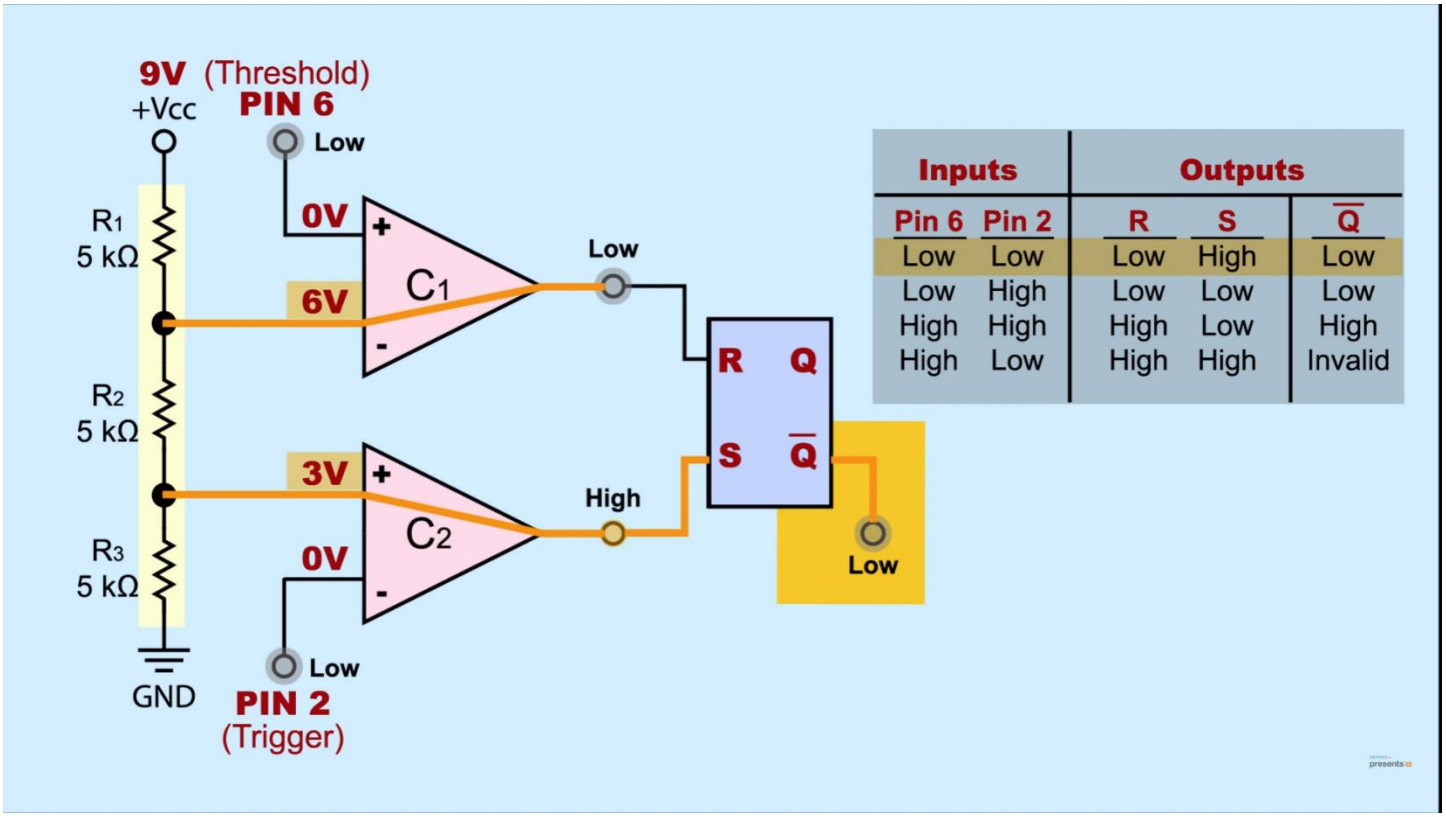



*Figure 2-6: The S-R Flip-Flop is SET because pins #2 and #3 are below their respective thresholds.*

Since the trigger (pin 2) is less than the 3V reference, it tells me the capacitor must be discharged since its voltage is less than 3V. In our case, that is because Vcc = 9V. If Vcc were 12V, the reference voltages would change accordingly. So, you see, the actual capacitor voltage is not what the 555 is monitoring. It is the *percentage* of charge that matters. That is why it can operate with a range of Vcc power. The trigger at pin 2 acts as a starter pistol that triggers the timer.

Now we need to see how the flip-flop is reset.

When the trigger is greater than its reference (3V), it causes the bottom comparator to output LOW. When the threshold goes above its reference of 6V it causes the top comparator to go HIGH and this RESETS the flip-flop and its output goes HIGH. The truth table highlights this condition.

Please note, at this point, we have used an analog signal to be processed by the 555 and only then does it output a *digital* signal that we can use in the rest of our circuit!

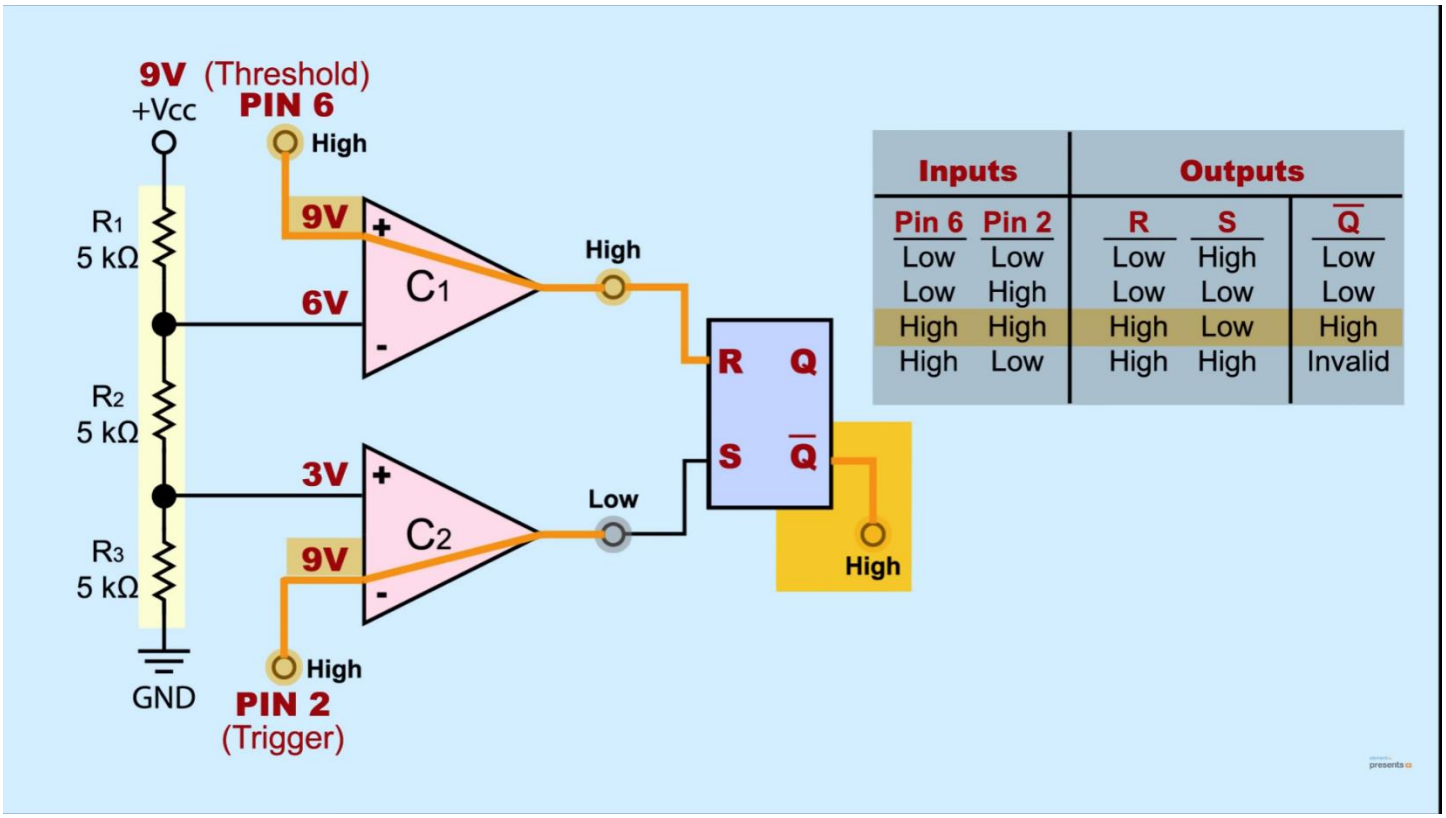



*Figure 2-7: The Flip-Flop is RESET when the threshold is high and the trigger is low.*

## Output Inverter

Now for the inverter bit. The green symbol in Figure 2-8 is called an inverter and it just changes a high digital signal to low and a low signal to high. This is exactly what would happen if we used the Q output of the flip-flop. But as we will see, there is a reason the 555 doesn't use the Q output.

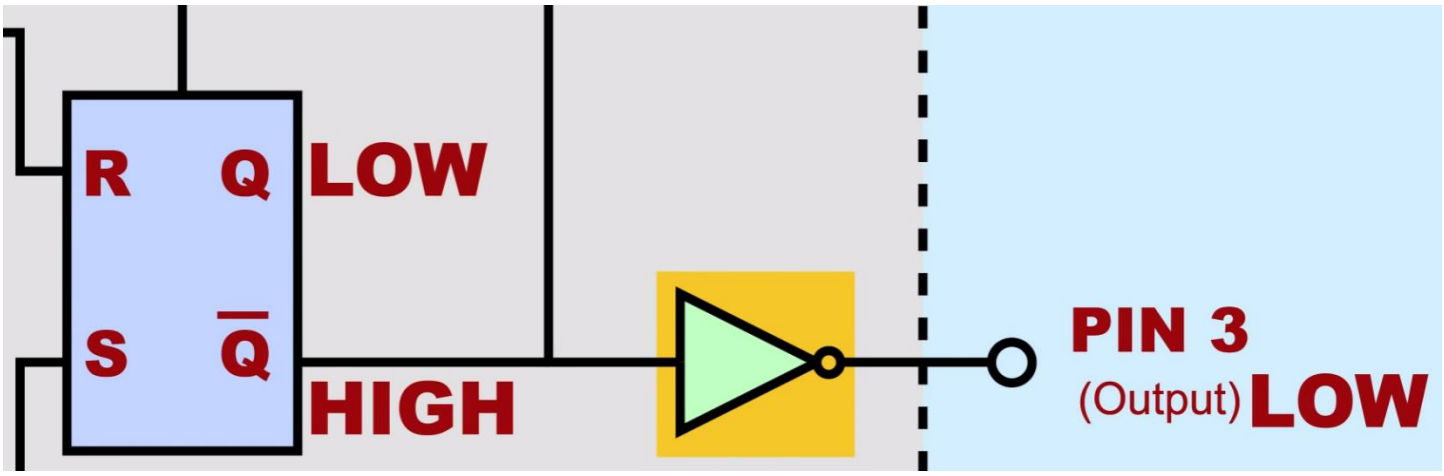



*Figure 2-8 An inverter is used to flip the output signal around so that a high is converted to a low, and visa-versa*

An inverter such as the 7404 IC is a common inverter chip. It is very simple to use. You connect a digital signal to its input and the opposite polarity signal appears at the output. However, instead of adding another IC to our circuit, we could use a NAND (7400) like we did in other projects. We would connect the two inputs and the opposite polarity signal comes out. This is handy when you have a spare NAND gate you are using on one of the chips on your board.

So, the inverter section makes the 555 behave like an *active on* device. After the inverter, SET outputs HIGH and RESET outputs LOW just like we are used to!

## Control Voltage (Pin 5)

We need to mention the control voltage option even though it isn't used very much. Pin 5 is connected internally to the negative pin of the top comparator as in Figure 2-9. This pin can be used to change the reference voltage which, in our case, is 6V.

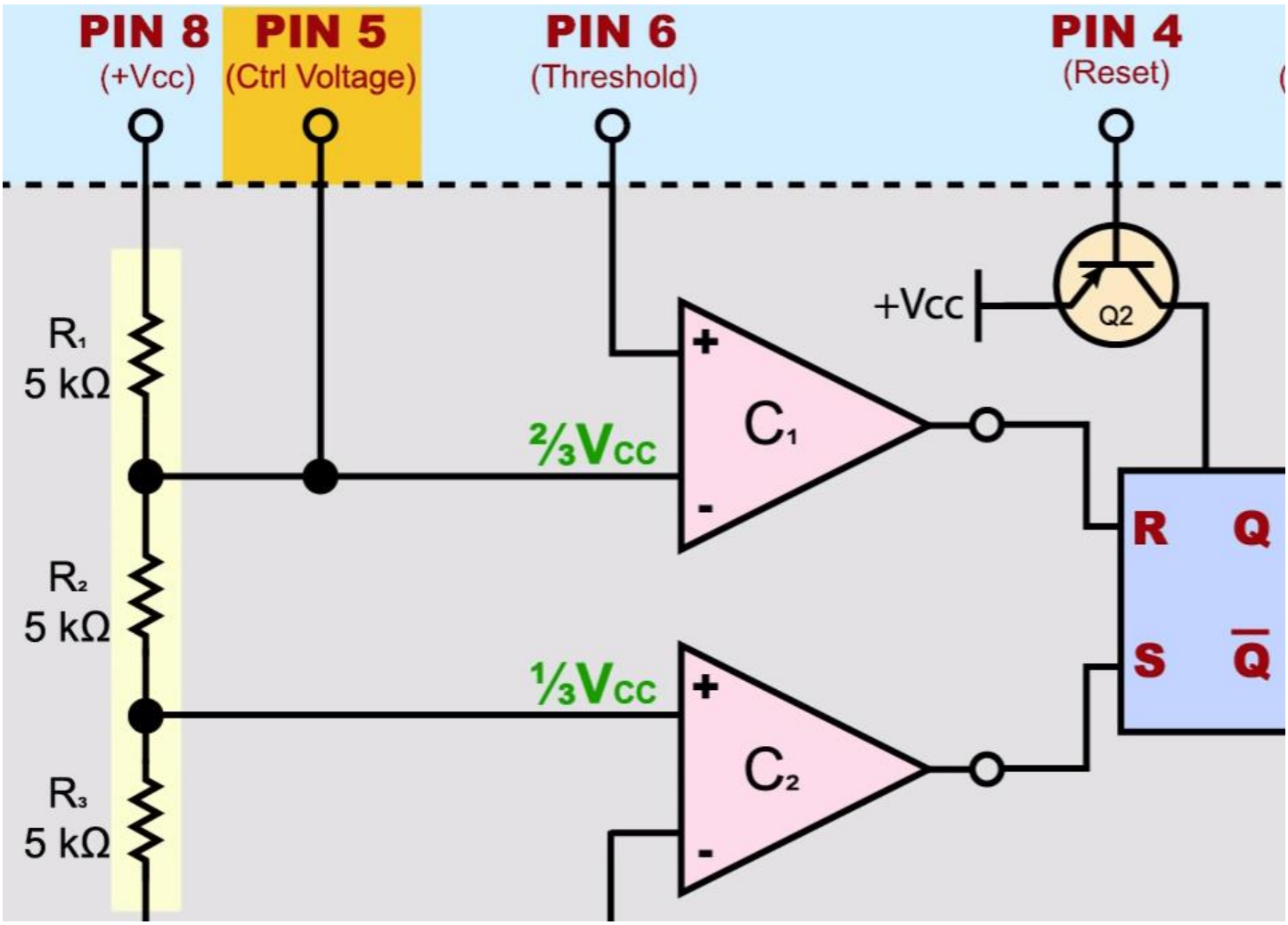



*Figure 2-9 The control pin can be used to change the voltage on the top comparators "-" input and change the threshold of the 2/3 level of a capacitor.*

## Reset (Pin 4)

Many times, it is desirable to have an easy way to reset the timer. That is what pin 4 is used for. You can see the reset pin is connected to the base of and PNP transistor (Q2). If an external switch (or signal from a microcontroller) is connected to ground, it turns on Q2 which provides a ground path through its collector and resets the flip-flop. Since a LOW signal turns Q2 on, its base is often pulled high by an external resistor. The configuration of control, threshold, trigger, and reset pins takes many forms because they are quite versatile.

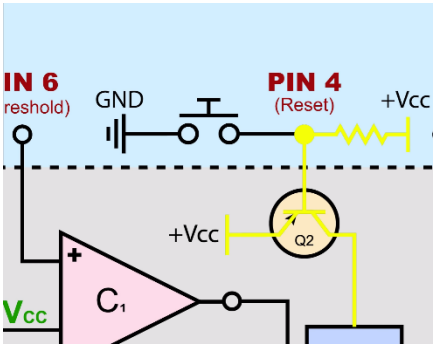



*Figure 2-10 Reset pin can reset the flip-flop through a PNP internal transistor (Q2)*

## Discharge (Pin 7)

The last pin we will examine is called the discharge pin. As its name implies, it is used to charge and discharge the external capacitor when one is connected. Figure 2-11 shows how it works.

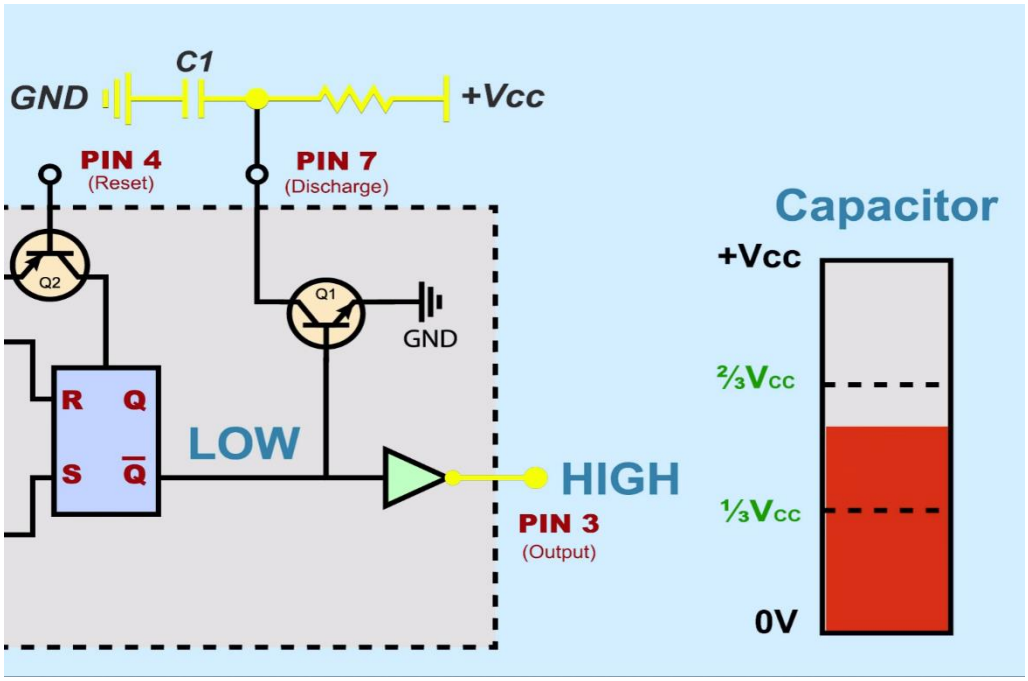



*Figure 2-11 The discharge is usually tied high to Vcc and Q1 is OFF when the flip-flip is Low. this allows the external capacitor to charge.*

Pin 7 is pulled high to Vcc. That means it is *active low*. When the flip-flop is LOW, the inverter supplies HIGH output to the external capacitor which charges it.

When the flip-flop changes state and goes HIGH, it means the capacitor is 2/3 charged and this causes the flip-flop to change states again. When $\overline{Q}$ goes high it turns on Q1 (NPN) and this provides a path to ground. The capacitor is connected to pin 3 so when LOW, it discharges the capacitor. So in this case, pin 3 does double-duty and both charges and discharges the external timing capacitor. Very clever! I should note that since the capacitor does not discharge through a resistor, it discharges almost instantly. We saw that in the scope image way back in chapter 1 (Figure 21).

Now its time to build our circuits!